Equation (5.22) - Transfer function for the variation of the clamp voltage in response to direct current injection in the clamp capacitor: the transfer function describing the response of the clamp voltage control system to a variation of the net current injected in the clamp capacitor can be obtained, according to the principle of superposition, by neglecting the clamp voltage reference input in Fig. III.1 and taking the disturbance input ΔI_c^d as the main system input. The resulting transfer function can be written as:

$$\frac{\Delta V_c(s)}{\Delta I_c^d(s)} = \frac{G_{clamp}(s)}{1 + G_{PI}(s) \cdot G_{clamp}(s)} = \frac{\left(\frac{1}{sC_c}\right)}{1 + k_p\left(1 + \frac{1}{sT_i}\right)\left(\frac{1}{sC_c}\right)}.$$

If this transfer function is reduced to the standard form, then equation (5.22) is obtained:

$$\frac{\Delta V_c(s)}{\Delta I_c^d(s)} = \frac{sT_i/k_p}{1 + sT_i + s^2\frac{T_i C_c}{k_p}}.$$

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enables a considerable increase of the converter's power density, if the soft-switching converter is operated with the same mean switching frequency and the same junction temperatures as the hard-switched one, because the soft-switching converter would then require a much smaller heat sink. Alternatively, the soft-switching converter can be designed to operate at a mean switching frequency above the audible region, having roughly the same size as a hard-switching converter which operates with a five times lower mean switching frequency. The soft-switching converter also exhibits a lower rate of change of the voltage (dv/dt) at the switching instants, which is beneficial to the insulation of the machine windings and causes lower radiated EMI.

An experimental verification of the values which have been theoretically calculated in chapters 5 and 6 has not been possible with the test rig used and within the time frame of this work. Therefore, the following issues are suggested for further work:

- experimental determination of the maximum attainable power density of the SRM;
- redesign of the ACRDCL SR converter for maximum power density and evaluation of the actually attainable power density;
- experimental determination of the efficiency for the whole drive system for different operating conditions;
- development of an active input rectifier for the ACRDCL SR converter and of a single control unit for synchronized operation of the input and output stages.

vices employed. It depends only on the natural frequency of the resonant tank and on the current magnitude at the end of the boost phase, i.e. on the boost factor. The maximum value of dv/dt at the DC link voltage transitions can be found from equation (5.5) to be given by:

$$\left(\frac{dv}{dt}\right)_{max} = \omega_r \, V_s \sqrt{1.0+k_b^2}. \tag{6.6}$$

For a boost factor of 1.0 and a supply voltage of 500V, the maximum IEC specification would be met if the natural frequency of the resonant tank is lower than approximately 110 kHz, yielding a dc link frequency of approximately 70 kHz for a clamp factor of 1.5. The reduced dv/dt at the DC link transitions would also contribute to a reduction of the radiated EMI produced by the converter. With respect to the conducted EMI, if the DC link is fed by a diode rectifier with large DC link filter capacitance, no significant improvement can be expected, as has been verified in [22] for other soft-switching converter topologies. In this case, the large DC link filter capacitance practically decouple the input rectifier from the rest of the converter, so that it is relatively irrelevant if a hard- or a soft-switching converter is used in the output stage. However, the input current is very distorted, with poor power factor and high harmonic content if a diode rectifier is used in the input stage. As more and more rigorous standards for energy quality are prescribed, it is likely that diode input rectifiers become unacceptable due to input EMI filtering requirements. A potential substitute for diode rectifiers would be an active rectifier with control of the input current (Fig. 6.3). If this kind of rectifier is used with ACRDCL converters, then the zero-voltage notches of the resonant DC link can be also used to commutate the input switches under ZVS conditions. Additionally, regeneration is also possible with this topology.

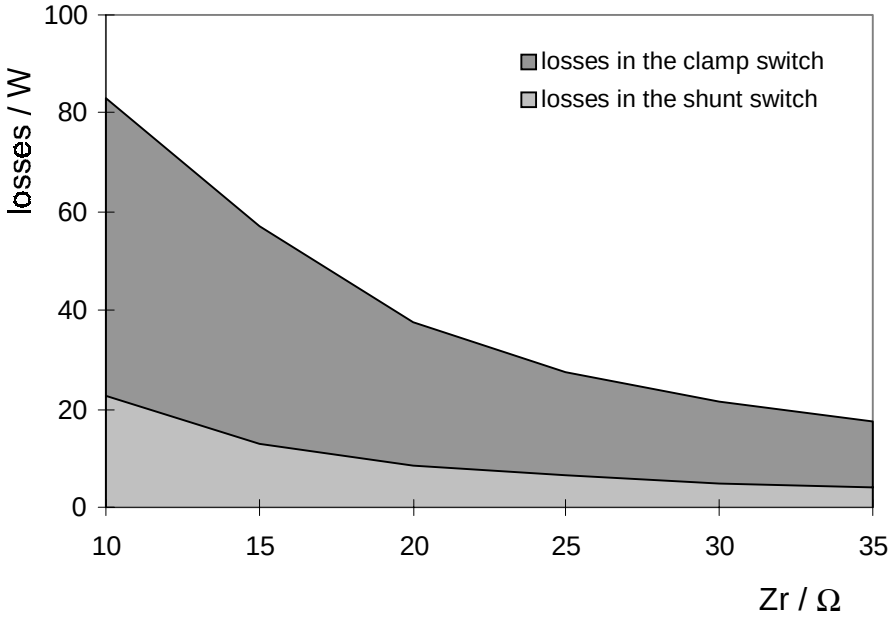


Fig. 6.2: Losses in the DC link switches versus characteristic impedance for fixed DC link frequency (80kHz).

The variation of the losses in the resonant inductor for different values of characteristic impedance is more difficult to predict. There are many possibilities for the construction of the resonant inductor, and each design parameter has a more or less strong impact on the inductor losses and on the inductor size. For instance, Sommer [89] has shown that the no-load losses in a resonant inductor with a ferrite core become lower if the inductance is increased. For a fixed natural frequency, the characteristic impedance of the resonant tank is directly proportional to the inductance. Therefore, the peak inductor current and the peak stored magnetic energy will be inversely proportional to the inductance:

$$I_{max} \propto \frac{V_s}{\omega_r L_r} \quad \therefore \quad E_{max} \propto 0.5 \left(\frac{V_s}{\omega_r}\right)^2 \frac{1}{L_r}. \tag{6.5}$$

If the magnetic core is designed to avoid saturation, i.e. for operation in the linear region, then the RMS value of the magnetic flux in the core will be approximately inversely proportional to $\sqrt{L_r}$, and the core losses will vary accordingly. If the core is not modified, then increasing the inductance by a factor

discrete power semiconductor devices and air-cooled heat sinks are used. The negative values in Table 6.3 indicate that the heat sink would have to be kept at a temperature below the ambient temperature, and this is not possible with natural air cooling. In contrast, it would be possible to implement the soft-switching converter using discrete devices for mean switching frequencies up to 30 kHz. Hence, operation of the soft-switching converter above the audible frequency region would be possible with a forced air-cooled heat sink, but the size of the heat sink would probably be very large. It is difficult to predict the size of the heat sink exactly, because the effective thermal resistance of an air-cooled heat sink depends on several factors, like the contact area between the power semiconductor devices ant the heat sink surface, the shape of the fins, the air flow speed between the fins and many others. Nevertheless, some typical values of volumetric thermal resistance for air-cooled heat sinks under different flow conditions are presented in Table 6.4, which has been taken from reference [49].

Table 6.4: Volumetric thermal resistance (cm^3K/W) of air-cooled heat sinks.

flow condition (m/s)	*volumetric thermal resistance (cm^3K/W)*
natural convection	500-800
1.0	150-250
2.0	80-150
5.0	50-80

If power modules were used instead of discrete devices, it would be possible to operate the hard switched converter at a mean switching frequency above the audible region. However, it would require an air-cooled heat sink which would be twice as large as the one that would be required to operate the soft-switching converter at the same frequency. In this case, there would be a significant gain in power density if soft switching is used, because the heat sink itself represents a considerable part of the total converter's weight. In this design

The switching losses for the soft-switching case in Table 6.2 have been calculated under the assumption that the ZVS losses in IGBTs are 1/6 of the hard-switching losses. In fact, the ZVS losses depend strongly on the rate of rise of the collector-emitter voltage at turn-off. This in turn depends on the natural frequency of the resonant tank and on the "trip" current level at which the shunt switch in the DC link is turned off. As already mentioned above, the switching loss reduction rate of approximately 1/6 has been experimentally determined for second-generation IGBTs from both (low saturation and fast switching) types and is valid for a natural frequency of approximately 80kHz, which yields a DC link frequency of approximately 50 kHz if the clamp factor is 1.5. In the case where the sampling frequency (DC link frequency in the soft-switched converter) is 100 kHz, the required resonant frequency is approximately 150 kHz. In this case, the switching loss reduction is somewhat lower and lies between 1/5 and 1/4 for second-generation fast-switching IGBT devices. In order to evaluate the influence of the loss reduction due to soft-switching on the converter size, some design options are discussed next.

6.3 Converter sizing

If one wishes to construct SR converter like the one that has been simulated, there are two possibilities for the choice of the IGBT devices. First, one may choose to construct the converter using discrete components. Suitable IGBTs and diodes for the power level in question are encapsulated in a TO-247 package, which weights just 6g and can dissipate up to 78W at a maximum case temperature of 100°C (considering a maximum junction temperature of 150°C). The total weight of the semiconductor devices in the output section would be then just 72g. Alternatively, one may use chopper power modules consisting of one IGBT and one diode, which weigh 150g and can dissipate up to 180W under the same conditions as above, because they have a better thermal interface to the heat sink. In this case the total weight of the semiconductor devices would be 900g. For the purpose of comparing the resultant heat sink sizes in each case, the required thermal resistance of the heat sink to ambient

The conduction and the switching losses in the IGBT devices have been calculated using the conduction and the switching models presented in [36], for a 1200V, 50A fast switching IGBT. The losses due to reverse recovery and the switching losses in the diodes have been neglected. The conduction losses in the diodes have been calculated by interpolation of the forward voltage drop versus forward current characteristics from the diode's data sheet. The model equations are summarized as follows:

IGBT on-state voltage drop: $$v_{CE} = (V_0 + V_1\,T) + (a_0 + a_1\,T)\cdot i_c^{(b_0 + b_1\,T)}; \quad (6.1)$$

IGBT turn-on energy loss: $$E_{on} = (h_0 + h_1\,T)\cdot i_c^{(k_0 + k_1\,T)}; \quad (6.2)$$

IGBT turn-off energy loss: $$E_{off} = (m_0 + m_1\,T)\cdot i_c^{(n_0 + n_1\,T)}; \quad (6.3)$$

diode forward voltage drop: $$v_f = V_F + c\cdot i_f^{\,d}\,; \quad (6.4)$$

where T is the junction temperature in °C. The diode model parameters have been calculated from data sheet characteristics for a fixed junction temperature of 100°C.

If the soft-chopping control method is used, the partitioning of the total power losses in conduction and switching losses is quite different in the soft-chopped SRM converter, when compared to a converter for induction motor drives. This is due to the fact that only the upper switches are pulsed in the soft-chopping SRM converter. The lower switches are turned on and off only one time for each phase current pulse. As a result, the lower switches will exhibit practically only conduction losses, while the switching losses in the upper switches can be higher than the conduction losses (see Table 6.1). The relative distribution of the loss components on the semiconductor devices is shown in Table 6.2 for mean switching frequencies of 7.5, 15 and 30 kHz, which correspond to the sampling frequencies of 25, 50 and 100 kHz, respectively.

Table 6.1: Average switching frequency and conduction losses for one phase of an asymmetric-bridge SR converter.

f_s *kHz*	$\overline{f}_{sw}$ *kHz*	P_{sh} *W*	P_{sl} *W*	P_{dh} *W*	P_{dl} *W*	P_{sw} *W*	P_{total} *W*
20	6	33.5	49.2	6.3	21.2	21.8	132.0
25	7.5	33.1	49.6	5.9	21.6	27.0	137.2
40	12	33.4	50.0	6.0	21.8	42.6	153.8
50	15	33.6	50.0	6.2	21.7	53.0	164.5
100	30	33.6	50.2	6.1	21.8	104.0	215.7

The mean switching frequency shown in column 2 of Table 6.1 has been computed by dividing the number of switchings in a current pulse by the duration of the dwell period. The power values shown in columns 3–6 of Table 6.1 are the conduction losses in the various components of the asymmetric bridge converter, which are identified in Fig. 6.1. Simulation results showing the currents on the branches of the asymmetric bridge for a sampling frequency of 25 kHz are also shown in Fig. 6.1.

- the high radial forces acting on the pole tips of stator and rotor can also give rise to mechanical vibrations and cause premature bearing failure at high power levels.

On the other hand, a SRM drive could be an economical replacement for low-power drive systems using motors which also have inherently high torque pulsations, e.g. single-phase induction motors or universal motors. However, the use of soft-switched SR drives seems to be more attractive in medium power ranges starting at some tens of kW, where the costs of sensors, control circuits, additional components and power electronic devices have a lower weight in the overall costs of the drive system, in comparison with a low-power system. For this reason, the considerations that follow and the simulation results which are presented in this section refer to systems of medium power level.

6.2 Optimization of the drive circuit

Depending on the application, it may be more important to enhance other qualities of the ACRDCL SR converter. For instance, if a highly dynamic current control is aimed, one may want to maximize the switching frequency of the main switches in the output stage. A reasonable limit for the switching frequency would be the frequency for which the overall converter losses become equal to the losses of a hard-switching converter of same power rating. In this extreme case, there would be no gain in efficiency, and the cooling should be equally designed for both converters. As a general guideline, it can be assumed that the total switching energy of the power semiconductor devices in an ACRDCL circuit is roughly six times lower than the switching energy of the same devices in a hard-switched converter. This value has been derived from thermal measurements with second-generation IGBT devices [89], operating with a dV/dt value of approximately 400V/µs at turn-off. It is found to hold true within ±10% for IGBT devices optimized for low conduction losses as well as for devices optimized for faster switching speed. A comparable value of switching loss alleviation is also verified for MCT devices for a turn-off dV/dt of approximately 200V/µs [77].

The input and output power of the converter have been measured with a precision high-frequency power meter, for operation in current-regulated mode with a single-phase passive RL load. The efficiency has been then computed and the results are shown in Fig. 5.34.

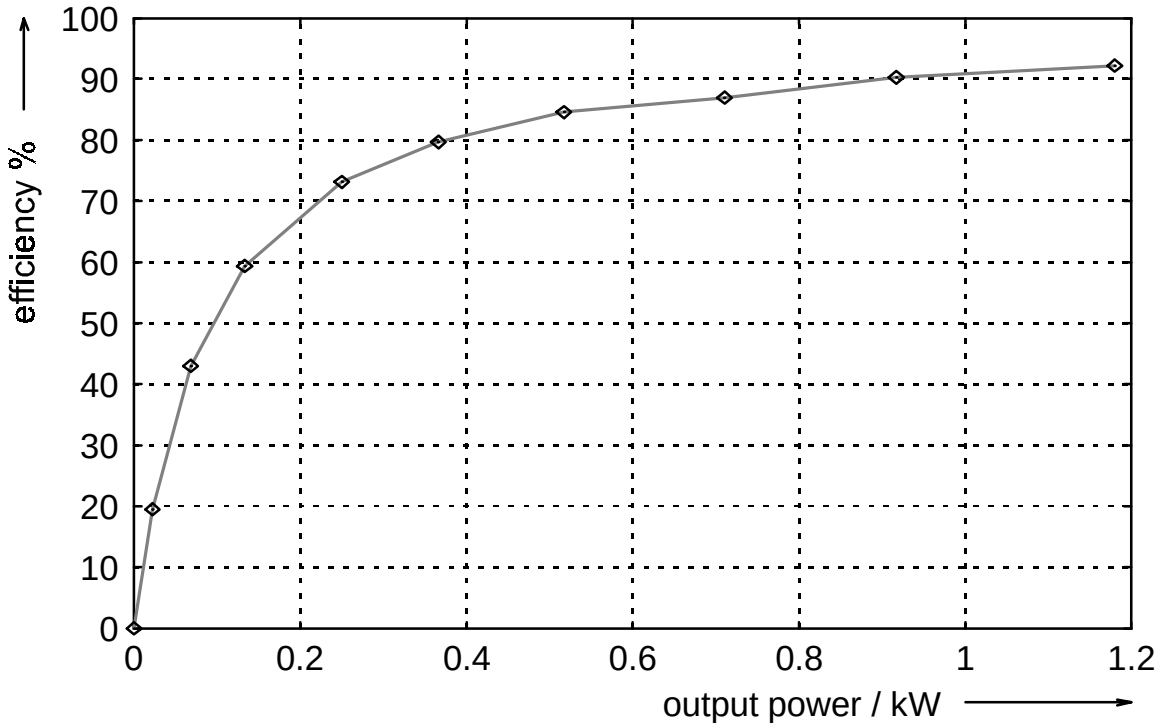


Fig. 5.34: Converter efficiency with passive load.

The measured total power losses remained approximately constant for the whole output power range considered. This indicates that the power losses in the passive components and on the auxiliary power semiconductor devices in the DC link are dominant with respect to the power loss on the main semiconductor devices in the output section. One reason for this has been the choice of MCTs as main devices. MCTs are commercially available only for current ratings above 65A. At currents under 5A, as was the case in the test circuit, the MCT switching losses are negligible, and it is therefore not possible to measure any reduction of main device switching losses at this current level. A direct comparison between efficiency in the ACRDCL SR converter and in a hard-

bility, and a limit of 2A has been set for the phase currents, in order to avoid instability of the clamp voltage during braking. As a result, the response is considerably underdamped and somewhat sluggish. The measured speed reversal exhibits a good agreement with the simulation results shown in Fig. 5.25.

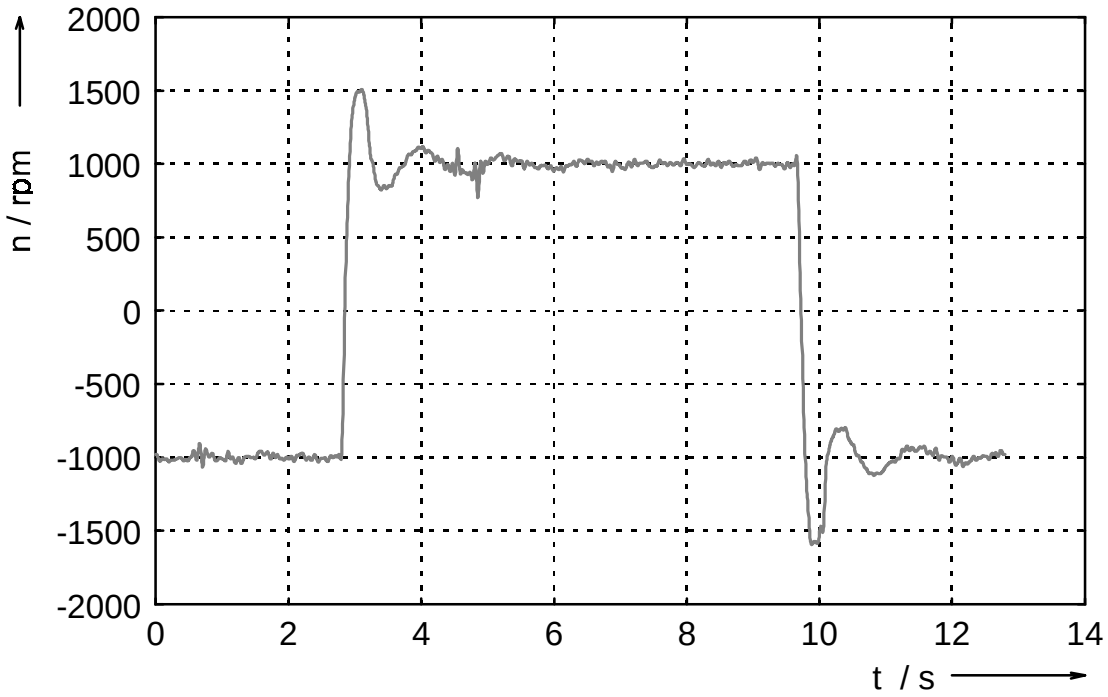


Fig. 5.31: Speed reversal at no load (measurement results); total shaft inertia $J_{SRM} + J_{DC} = 6.4 \times 10^{-4}$ kg·m^2.

Phase current and voltage waveforms for operation at regenerative braking are shown in figures Fig. 5.32 and Fig. 5.33. During braking operation, the phase current can only be controlled by hard-chopping. The output section injects thereby more energy in the clamp capacitor, which has to be returned to the source through the clamp switch and the resonant inductor. This is achieved by increasing the clamp turn-off current. If the maximum value of the clamp current is limited, there is also an upper limit for the braking current, which can be handled by the clamp circuit without causing instability of the clamp voltage. This limit depends on the size of the clamp capacitor, on the maximum allowable clamp turn-off current and on the dynamic response of the clamp voltage controller.

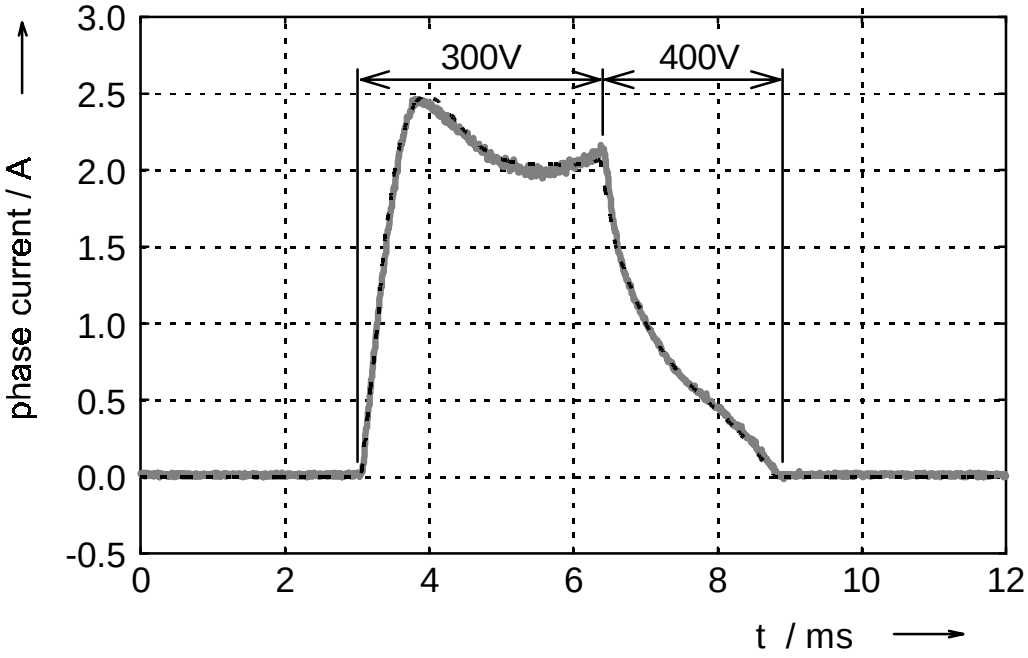


Fig. 5.28: Comparison of measured and simulated (dashed) phase current for single-pulse operation at 1500 rpm.

The test circuit has been operated in the current-regulated delta-modulation mode, with a sampling rate of approximately 25 kHz. The phase current and voltage for operation in this mode are shown in figures Fig. 5.29 and Fig. 5.30, for a load torque of approximately 0.5 Nm at 1500 rpm. The resulting mean switching frequency of the main switches in the output section, and the resulting current ripple for this operating mode, depend on the back-emf of the SRM. This, in turn, depend on the phase current level and on the machine speed. For the operating conditions mentioned above, the mean switching frequency lies around 5 kHz.

trol has been implemented using only one current sensor. The sensor is connected to the circuit in such a way, that the phase currents flow through it only during the dwell period or during free-wheeling. However, this phase current control method is somewhat restrictive if the motor is operated with dwell overlap. For this reason, the motor has been operated with a fixed dwell angle of 30° (no dwell overlap) and with the optimum turn-off angles determined in section 5.4.3.

Fig. 5.27 shows the measured voltage at the resonant DC link and the current throguh the resonant inductor, under no load, for a clamp factor of 1.2. The frequency of the DC link voltage under these operating conditions is approximately 25 kHz, in accordance to the value predicted by equation (5.20). The total no-load losses of the ACRDCL converter have been estimated as approximately 90 W. The validity of the simulation model can be verified by comparing these waveforms to the corresponding simulation results shown in figures Fig. 5.22 and Fig. 5.23. A good agreement between measurement and simulation can also be observed in the current waveforms shown in Fig. 5.28, which have been obtained for single-pulse operation at a speed of 1500 rpm. In both cases, the circuit has been supplied from the rectified single-phase 220V mains.

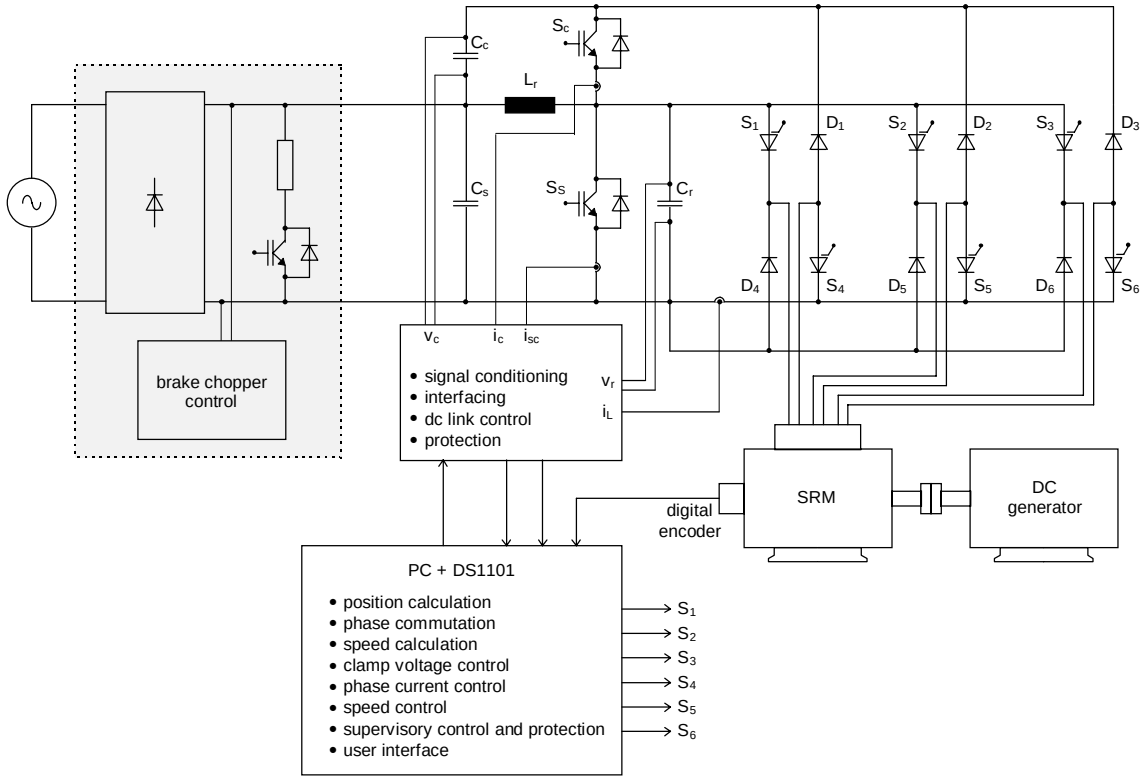


Fig. 5.26: Schematic diagram of the experimental setup.

The output section of the prototype ACRDCL SR converter uses MCTs as main switches. The other auxiliary switches in the circuit are realized with IGBTs. The lower on-state voltage drop of MCTs is very beneficial in an asymmetric-bridge SR converter. Since two switching devices are connected in series to each phase winding, the conduction losses should be as low as possible. With MCTs, the conduction losses can be reduced by as much as 50% with respect to other devices. On the other hand, the inability of the MCT in interrupting short-circuit currents is not critical in an asymmetric bridge SR converter, since the circuit topology itself eliminates the possibility of phase shoot-throughs.

In order to have a minimum of external hardware, most control functions have been implemented in software. Time-critical functions like phase commutation,

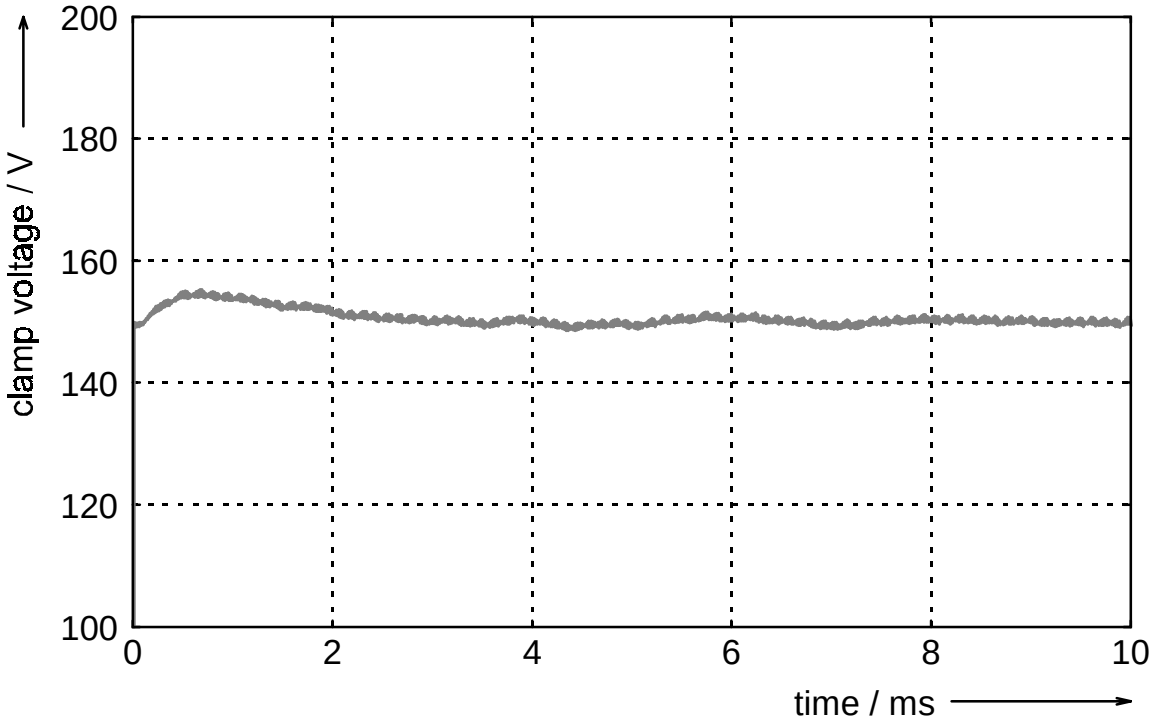


Fig. 5.24: Clamp voltage response to braking current starting at t=0 (simulation results).

Based on the above results, it can be stated that the braking capability of the ACRDCL SR converter is limited, because the regenerated energy flows through the clamp circuit. Therefore, the braking current must be limited, in order to keep the clamp voltage stable. The dynamic response of the whole drive system has been then simulated, taking into account the braking current limit. A purely inertial load has been used in the simulations, so that the braking capability of the drive system is emphasized, because of the absence of a braking load torque. A proportional + integral (PI) controller has been used for speed control, and its parameters have been set in such a way that the braking current limit is not exceeded. The simulated motor response to a reversion of the speed reference signal from -1000rpm to 1000rpm is shown in Fig. 5.25.

resonant inductor: L_r = 60µH,
resonant capacitor: C_r = 47nF,
clamp capacitor: C_c = 47µF.

The circuit has thus the following characteristic quantities:

natural frequency: $f_r \approx 95$ kHz
characteristic impedance: $Z_r \approx 36\ \Omega$

Simulation results showing the voltage across the resonant capacitor, i.e. the resonant DC link voltage, and the current throguh the resonant inductor under no load are shown in figures Fig. 5.22 and Fig. 5.23.

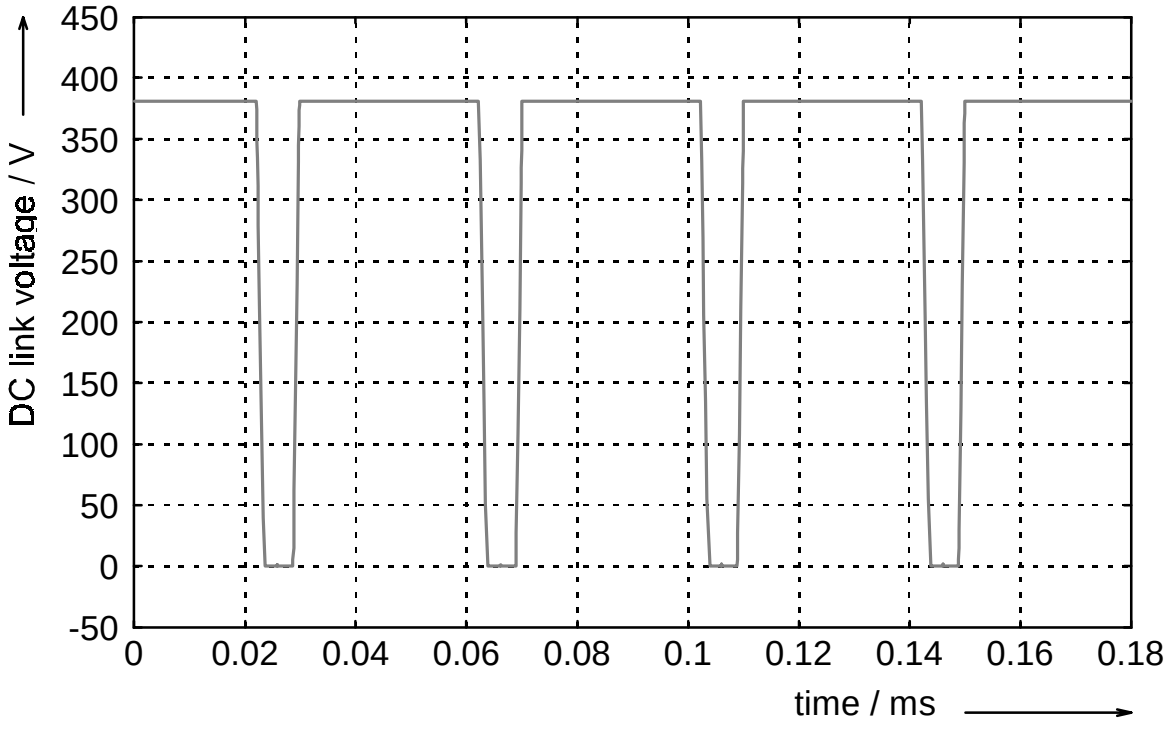


Fig. 5.22: Resonant DC link voltage (simulation result).

Fig. 5.20 shows running torque waveforms for different current levels, using the optimum commutation angles found above for the speed of 1000 rpm. The relationship between the reference current value and the mean torque for the same conditions as above is shown in Fig. 5.21.

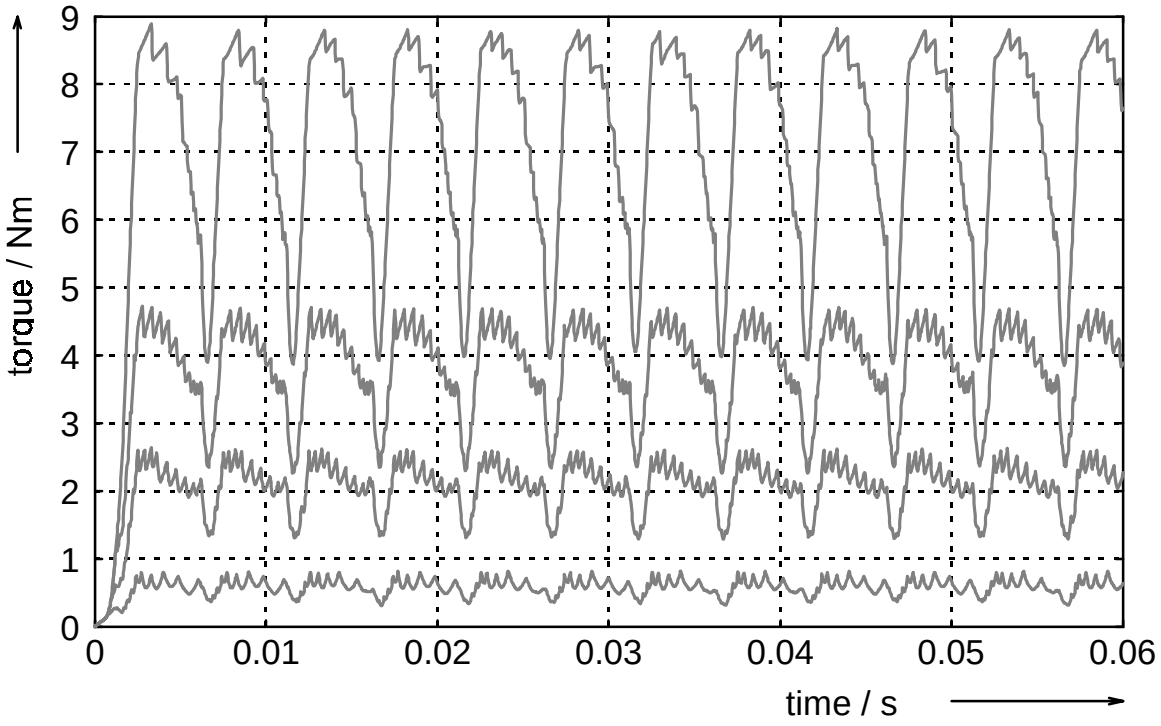


Fig. 5.20: Running torque waveforms at 1000rpm for constant current references of 1A, 2A, 3A and 5A, from bottom to top (simulation results).

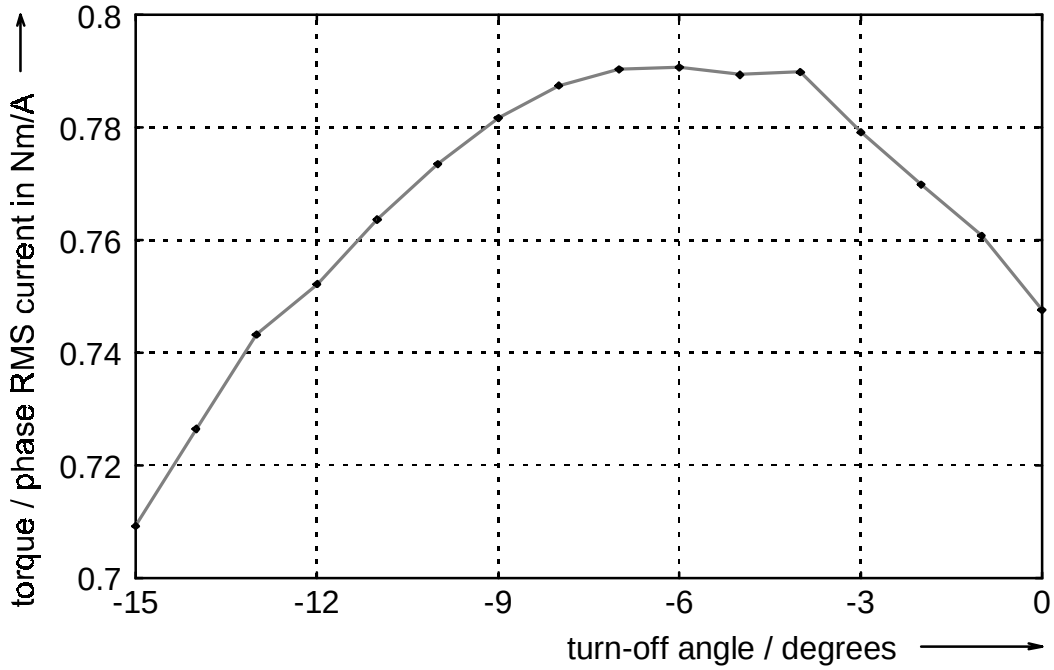


Fig. 5.16: Torque per phase RMS current versus turn-off angle at 500rpm, for fixed turn-on angle (-45°) and for constant current reference (5A) (simulation results).

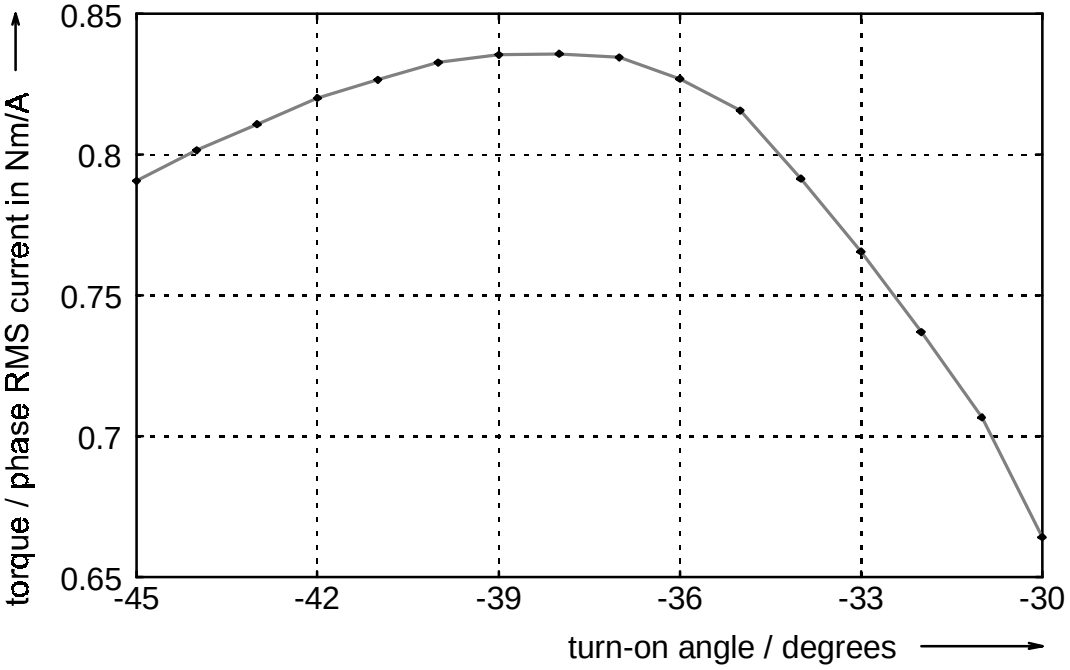


Fig. 5.17: Torque per phase RMS current versus turn-on angle at 500rpm, for optimum turn-off angle (-6°) and for constant current reference (5A) (simulation results).

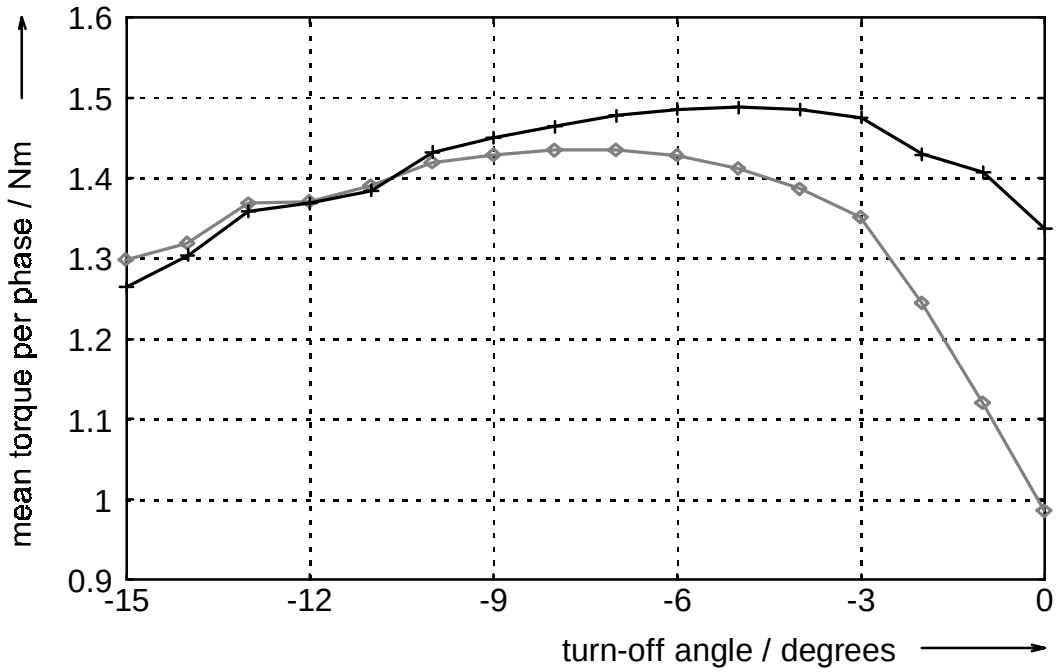


Fig. 5.14: Absolute mean torque produced by one phase versus turn-off angle, for single-pulse operation with fixed turn-on angle (-45°) at 1500 rpm: (o)=conventional SR converter; (+)=ACRDCL SR converter with k_c=1.5 (simulation results).

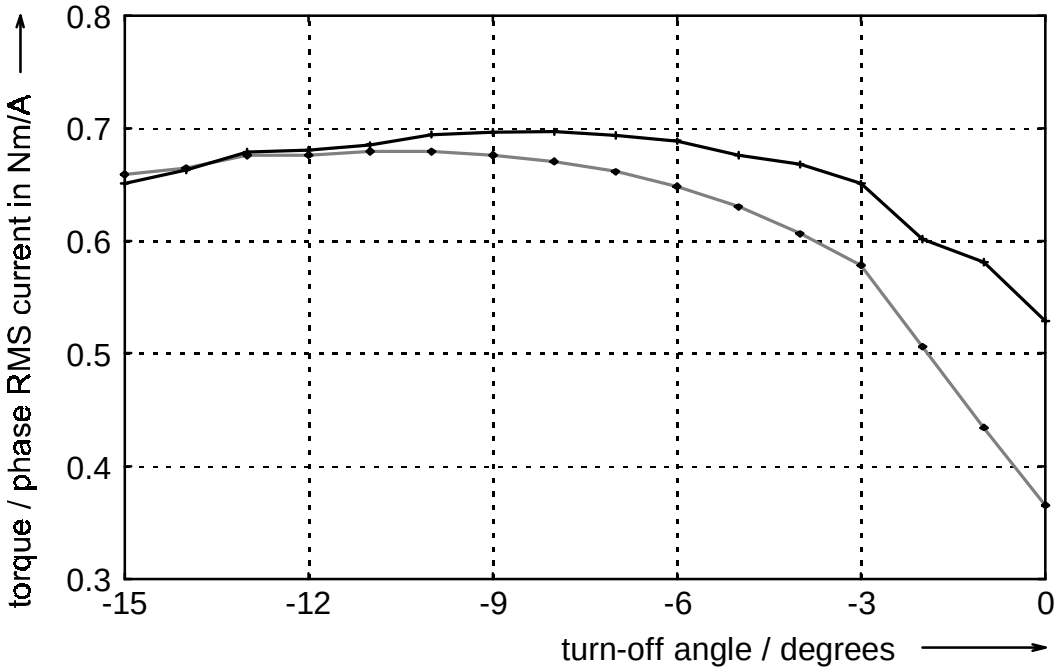


Fig. 5.15: Specific torque (Nm/A_{RMS}) produced by one phase versus turn-off angle, for single-pulse operation with fixed turn-on angle (-45°) at 1500 rpm: (o)=conventional SR converter; (+)= ACRDCL SR converter with k_c=1.5 (simulation results).

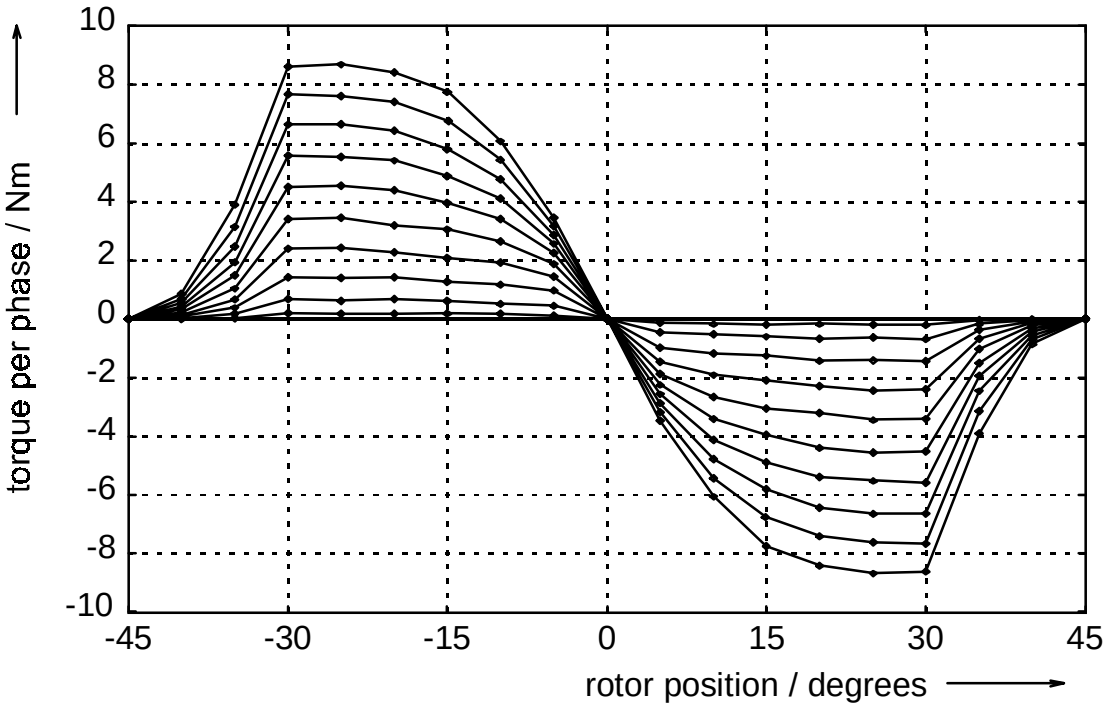


Fig. 5.12: Measured static torque produced by one phase versus rotor position, for currents varying between 0 and 5A in 0.5A steps.

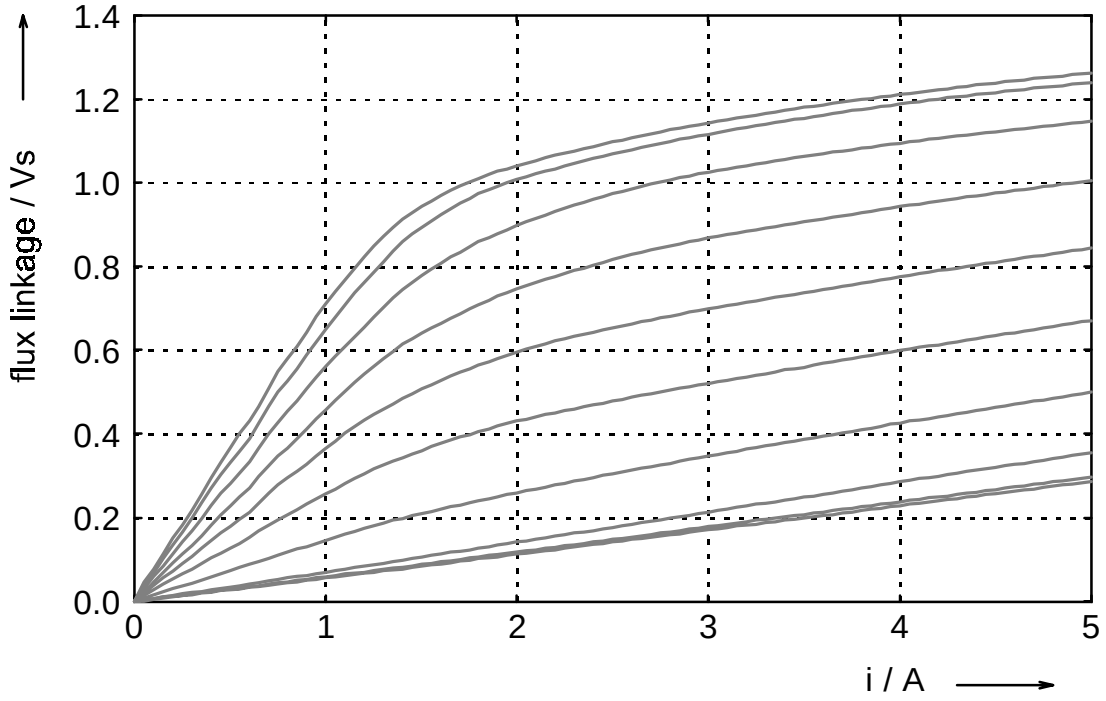


Fig. 5.13: Measured flux linkage of one phase versus current, for positions varying between -45° and 0° in 5° steps.

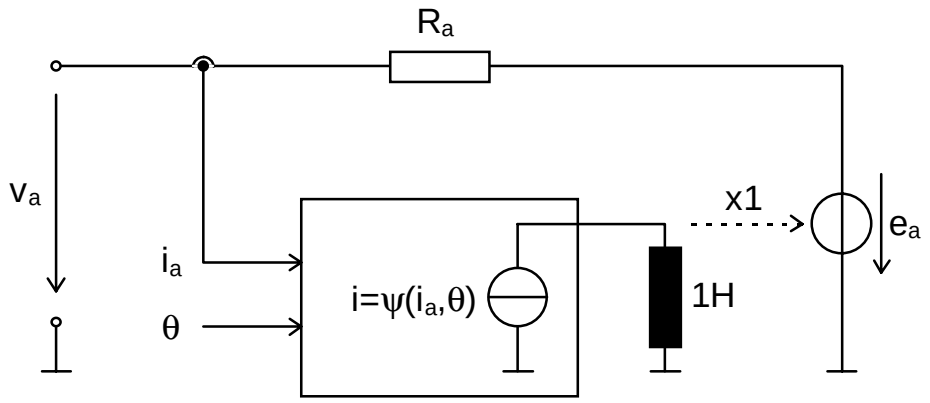


Fig. 5.11: SPICE model for calculation of counter emf for one phase of a SRM.

The structure shown in Fig. 5.11 should be repeated for each phase. Similar subcircuits should also be used to compute the running torque waveforms from the static torque data. The torque contributions from each phase can be then summed up at a common node and integrated by a capacitor connected to the same node. The voltage across this capacitor will be then proportional to the shaft speed.

To keep the computer memory requirements low, the characteristics used in the subcircuits can be tabulated for one electrical half-cycle only. The machine is assumed to be symmetrical, so that the same basic characteristic is used for all phases. The tabulated torque and magnetization data are given in Appendix II. The position information, obtained by capacitive integration of the speed signal, must be remapped to the angle region for which the torque and magnetization characteristics are tabulated, with the due displacements for each phase.

For the power electronic part of the system, simplified quasi-ideal switch models have been used. The use of more accurate models, like that described in [5], for example, demand much longer computing times than an ideal switch model. Therefore, such accurate models are more appropriate for simulation of just a few switching cycles, with the purpose of investigating worst-case device voltage and current stresses. In that case, only the switch itself and a part of the circuit around it need to be modelled in detail. Simulation of low-

The effect of the higher demagnetization voltage provided by the clamp rail over the torque production has been investigated with help from numerical simulations, which are discussed in the following section.

5.4 Simulation

The simulation of the ACRDCL SR converter has been executed with the program SPICE, developed at the University of California in Berkeley [102]. The program is public-domain and freely obtainable from the Internet. The current version, that has been used in this work, is version 3f4. SPICE is a circuit-oriented analog simulator, i.e. all system components, including controllers, switching control logic and electromechanical subsystems must be described in terms of analog equivalent circuits. These in turn consist on a netlist, containing linear and non-linear analog electric element models. The system is solved using trapezoidal integration with self-adaptive time step. Some commercial implementations of SPICE are also capable of mixed-mode simulation, including digital elements, and behavioral (i.e. transfer-function) models of controllers or other subsystems.

To simulate a complete SR drive system with SPICE, the user should provide a means for representing the highly non-linear magnetization characteristics of the SRM. At each time step, the torque and the counter emf should be computed for each phase, so that the motor equations (2.9) and (2.10) can be solved, as well as the equations for the remaining system. The on-line computation of torque and counter emf should be reasonably accurate and fast, to allow the simulation of lengthy mechanical transients in practical time. A good compromise between accuracy and computational speed is reached if some points of the static torque and magnetization characteristics are tabulated for different positions and current levels, and the actual instantaneous values are then obtained by on-line interpolation [25]. With SPICE, it is not possible to input such a two-dimensional look-up table directly. However, a sub-circuit structure which behaves like a linearly-interpolated look-up table can be de-

If a "hardness factor" for the clamping process is defined as:

$$k_h \triangleq \frac{C_c}{C_r}, \tag{5.29}$$

then the per unit peak variation of the clamp capacitor voltage can be expressed as:

$$\frac{\Delta v_{C_c\,max}}{(k_c - 1)\cdot V_s} = \sqrt{\frac{1 + k_h (k_c - 1)^2 + k_b^2}{(1 + k_h)\cdot (k_c - 1)^2}} - 1\,. \tag{5.30}$$

The clamp capacitance can now be selected by establishing an upper limit for the maximum variation of the voltage across the clamp capacitor. The relationship given by (5.30) is represented graphically in Fig. 5.9, as a function of the hardness factor, for a boost factor equal to 1.0 and for different values of clamp factor.

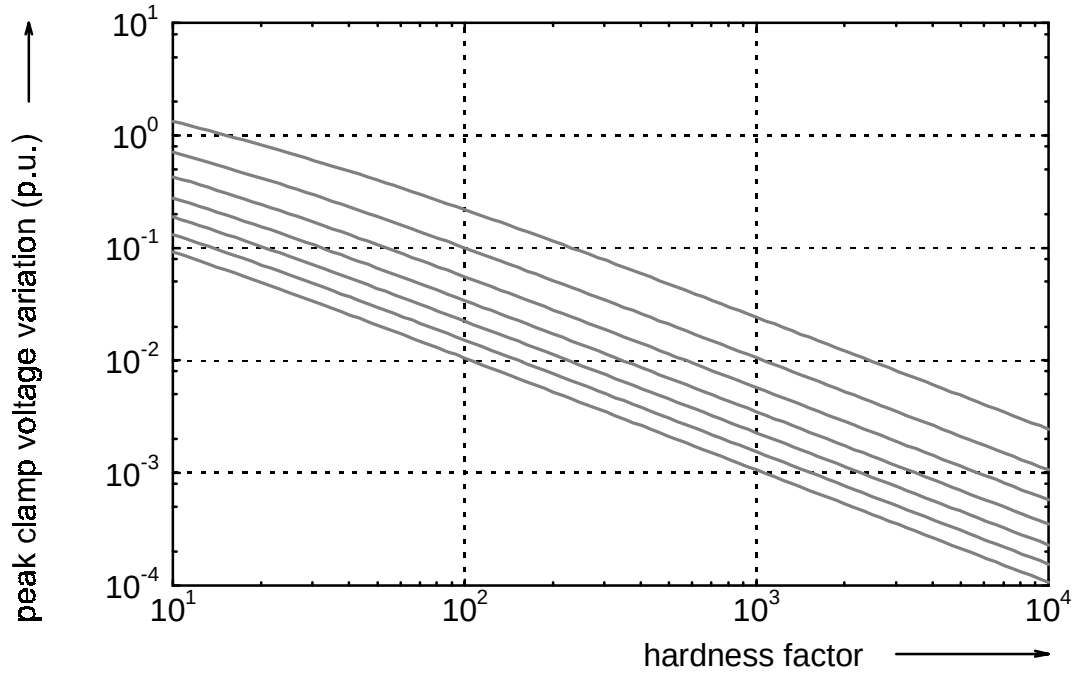


Fig. 5.9: Per unit peak variation of the clamp voltage versus hardness factor for k_b = 1 and k_c varying from 1.2 (upper trace) to 1.8 (lower trace) in 0.1 steps.

impedance, for a fixed natural frequency, will apparently reduce the overall losses, because the peak DC link current will be lower, causing lower conduction losses in the power semiconductor devices. However, the realization of a higher characteristic impedance at a given natural frequency requires the use of a larger resonant inductance and of a smaller resonant capacitance. Higher values of inductance generally imply larger inductor sizes and higher equivalent series resistance (ESR) values. The total inductor losses can thus be thought of as consisting of two components:

- the loss component associated to the resonant current, which is inversely proportional to the characteristic impedance;
- the loss component associated to the output current, which is directly proportional to the ESR and therefore increases for higher inductance or characteristic impedance values.

Based on the above considerations, it can be stated that there is an optimal value of inductance, and consequently of characteristic impedance, that minimizes the overall converter losses. A rough estimate of the optimum impedance can be obtained by modeling the DC link current as a high-frequency sinusoidal at the resonant frequency (amplitude V_s/Z_r) superimposed to a rectified sinusoidal at the DC link fundamental frequency (amplitude I_o). In this case, the overall inductor losses can be easily written as:

$$P_L = \frac{1}{2} ESR \cdot \left(I_o^2 + \frac{V_s^2}{Z_r^2} \right). \tag{5.24}$$

If the ESR of the resonant inductor is written as the product $Q \cdot L_r$, where Q is the quality factor of L_r , then the minimum of (5.24) can be found to occur for:

$$Z_r = \frac{V_s}{I_o} \ . \tag{5.25}$$

It has been verified empirically by some authors [75, 89] that the above relationship yields a good compromise between inductor size, overall power losses

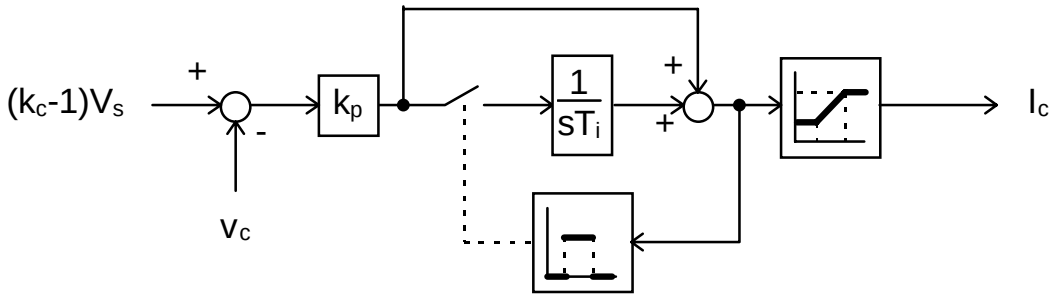


Fig. 5.8: Clamp voltage control.

If the clamp capacitance is large, so that the clamp voltage changes much slower than the DC link oscillation, then the current that flows into the clamp capacitor can be averaged, and its variation can be considered equal to the variation of the actuating signal I_c. In this case, the response of the clamp voltage to small variations of the clamp voltage reference is approximately governed by the following transfer function (Appendix III):

$$G(s) = \frac{1 + sT_i}{1 + sT_i + s^2 \dfrac{T_i C_c}{k_p}}. \tag{5.21}$$

The response of the clamp voltage control to sudden variations of the net current injected in the clamp capacitor, as occurs for instance when the motor is braked, is approximately given by (Appendix III):

$$\frac{\Delta V_c(s)}{\Delta I_c(s)} = \frac{sT_i / k_p}{1 + sT_i + s^2 \dfrac{T_i C_c}{k_p}}. \tag{5.22}$$

5.2 Design criteria

For the successful design of an ACRDCL converter, it is important to choose appropriate values for the natural frequency and for the characteristic imped-

$$I_o = \sqrt{I_c^2 - k_c(2 - k_c)\left(\frac{V_s}{Z_r}\right)^2}\,, \tag{5.17}$$

and this is the initial current for the boost period of the next cycle.

The period of the resonant DC link pulsation is given by the sum of the intervals (5.4), (5.8), (5.13) and (5.17):

$$T = T_{boost} + T_{rise} + T_{clamp} + T_{fall}\,. \tag{5.18}$$

If a "boost factor" k_b is defined as:

$$k_b = \frac{I_T}{(V_s/Z_r)}, \tag{5.19}$$

then, the DC link frequency can be found to be given by:

$$f = \frac{\omega_r}{2\left[k_b + \frac{\sqrt{k_b^2 + k_c \cdot (2 - k_c)}}{(k_c - 1)} + sin^{-1}\left(\frac{(k_c - 1)}{\sqrt{1 + k_b^2}}\right) - tan^{-1}\left(-\frac{1}{k_b}\right)\right]}. \tag{5.20}$$

A plot of the ratio between the DC link no-load frequency and the natural frequency of the resonant tank, as a function of the clamp factor and for different values of boost factor is shown in Fig. 5.7. In a typical application, the clamp factor would be, for instance, k_c=1.5 and the boost factor, k_b=1.0, yielding a DC link frequency equal to approximately 65% of the natural frequency f_r of the resonant tank. So, for typical f_r values of approximately 80 kHz, the DC link frequency would lie around 50 kHz.

$$v_{C_c}(t) = \sqrt{(k_c - 1)^2 V_s^2 + Z_r'^2 I_{co}^2}\, sin\left[\omega_r'(t - t_d) + tan^{-1}\left(\frac{(k_c - 1)V_s}{Z_r' I_{co}}\right)\right]; \quad (5.9)$$

$$i_c(t) = \sqrt{I_{co}^2 + \frac{(k_c - 1)V_s^2}{Z_r'^2}}\, sin\left[\omega_r'(t - t_d) + tan^{-1}\left(-\frac{Z_r' I_{co}}{(k_c - 1)V_s}\right)\right]; \quad (5.10)$$

where:

$$\omega_r' = \frac{1}{\sqrt{L_r(C_r + C_c)}}; \quad (5.11)$$

$$Z_r' = \sqrt{\frac{L_r}{(C_r + C_c)}}. \quad (5.12)$$

In the steady state, the final value I_c of the clamp current should be equal to the initial value I_{co} , so that the net charge transferred to the clamp capacitor is zero, keeping the clamp voltage regulated. If the clamp capacitor is large, the duration of the clamp period is approximately given by:

$$T_{clamp} \cong 2 \cdot \frac{|I_{co}| \cdot L_r}{(k_c - 1) \cdot V_s}. \quad (5.13)$$

falling resonant transition (from *f* to *a*)

The active path during the falling resonant transition is shown in Fig. 5.6. As in the case of the rising resonant transition, only the elements of the resonant tank are active. At $t = t_f$, switch S_c is turned off and the link current begins to be drained from the resonant capacitor C_r . The initial current in C_r will be the "trip" current value I_c , which was flowing through S_c at the end of the clamp period. The voltage v_{Cr} will then immediately start a falling oscillation, and this period ends when v_{Cr} reaches the zero voltage level, when D_s begins to conduct (instant ***a***), starting a new cycle.

The link voltage and current during this period can be written as:

$$v_{C_r}(t) = V_s + \sqrt{V_s^2 + Z_r^2 I_T^2}\ sin\left[\omega_r(t - t_c) + tan^{-1}\left(-\frac{V_s}{Z_r I_T}\right)\right]; \tag{5.5}$$

$$i_{L_r}(t) = \sqrt{I_T^2 + \frac{V_s^2}{Z_r^2}}\ sin\left[\omega_r(t - t_c) + tan^{-1}\left(\frac{Z_r I_T}{V_s}\right)\right]. \tag{5.6}$$

The duration of the rising resonant transition is given by:

$$T_{rise} = \frac{1}{\omega_r}\left[sin^{-1}\left(\frac{(k_c - 1)}{\sqrt{1 + \frac{Z_r^2 I_T^2}{V_s^2}}}\right) - tan^{-1}\left(-\frac{V_s}{Z_r I_T}\right)\right]. \tag{5.7}$$

clamp period (from ***d*** to ***f***)

The equivalent circuits for the clamp period are shown in Fig. 5.5. The diode D_c begins to conduct (instant ***d***) when the DC link voltage reaches the clamping level $k_c \cdot V_s$. While D_c is conducting (Fig. 5.5 (a)), the clamp switch S_c can be turned on under ZVS conditions. If the clamp capacitor is large enough, the link voltage v_{Cr} and the clamp voltage v_{Cc} remain approximately constant during the whole clamping process. In this case, the current i_{Lr} decreases almost linearly, until the clamp current i_c reverses and begins to flow through the switch S_c (instant ***e***, Fig. 5.5 (a)). S_c is kept closed until i_c reaches a preset value I_c , at which S_c is turned off, ending the clamp period. S_c is also switched off under ZVS conditions, because C_c and C_r do not allow a sudden change of the voltage at its terminals.

conducts the link current from the preceding cycle, which flows back to the DC supply. The magnitude of i_{Lr} decreases linearly thereby, under the influence of the supply voltage V_s . While D_s is conducting, switch S_s can be turned on under nearly zero voltage, with low turn-on losses. Eventually, i_s reverses and begins to flow through S_s (instant ***b***, Fig. 5.3 (b)). S_s is then kept closed for a short period of time, during which i_{Lr} is further linearly boosted. At a preset time after turn-on of S_s , or when i_s reaches a preset "trip" current level I_T , switch S_s is turned off (instant ***c***), ending the boost period. S_s is switched off at ZVS conditions, because C_r does not allow a sudden change of the voltage across it.

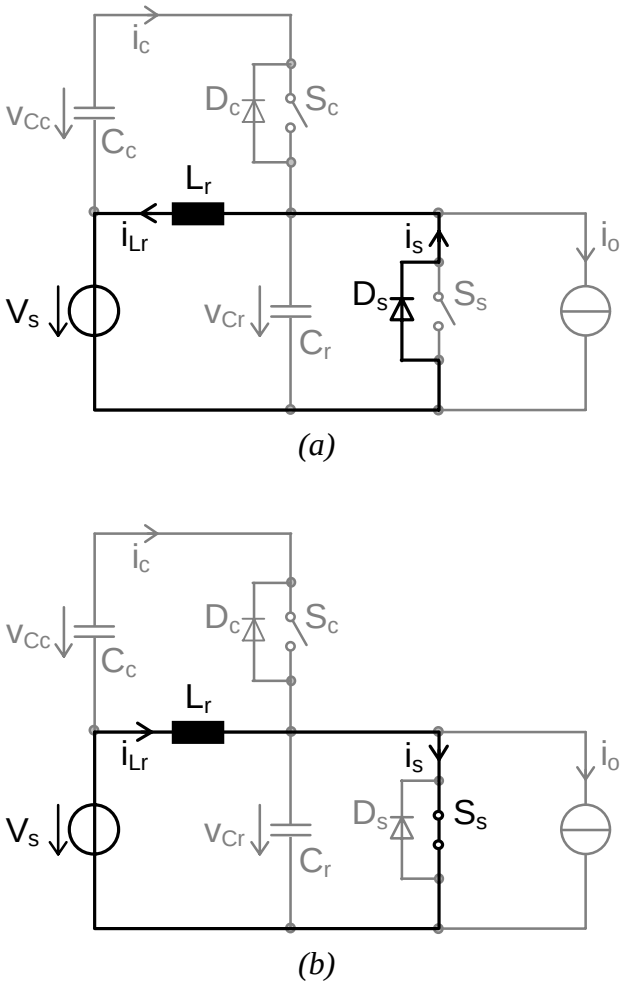


Fig. 5.3: Active paths during the boost period
*(a) between instants **a** and **b***
*(b) between instants **b** and **c***

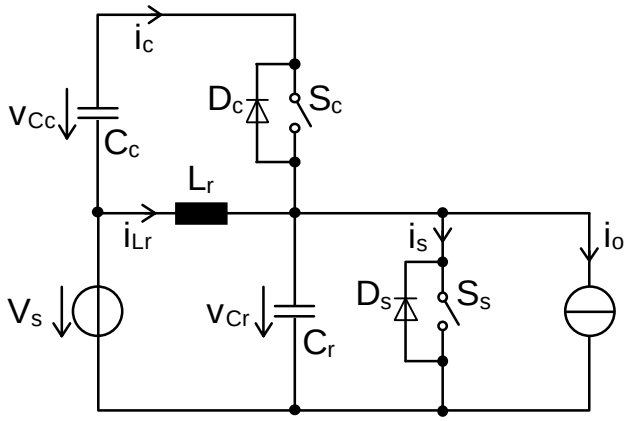


Fig. 5.1: Equivalent circuit for the ACRDCL.

The waveforms of the DC link voltage v_{Cr} and of the DC link current i_{Lr} , in steady-state under no load *($i_o = 0$)*, are shown in Fig. 5.2. One cycle of the DC link operation comprises a sequence of states, whose changes are characterized by the instants described in Table 5.1, also labelled in Fig. 5.2:

Table 5.1: Operating sequence of the ACRDCL.

instant	***state changes***
a	D_s conducts
b	D_s turns off, S_s conducts
c	S_s turns off
d	D_c conducts
e	D_c turns off, S_c conducts
f	S_c turns off

film capacitors. Another potential advantage of MLC technology is its suitability for integration, in the sense that is discussed in [88].

To illustrate the potential size reduction achievable by using the appropriate capacitor technology, a comparison between ceramic and electrolytic technologies is now presented. The data are taken from the clamp capacitor design for the ACRDCL SR converter, which is analyzed with more detail in chapter 5. Preliminary calculations show that the capacitor should have a capacitance value of 47μF at a working DC voltage of 150V. The RMS current ripple capability must be higher than 8.1A at 25kHz. If a single aluminum electrolytic capacitor is used, the smallest capacitor that matches the current ripple requirement has a capacitance of 2200μF (approximately 47 times higher than the required value) at a voltage rating of 200V, a volume of 20cm^3 and weights approximately 100g. The ESR is approximately 33mΩ, yielding a power loss of ca. 2W. Additionally, it is very likely that one or more film capacitors with low equivalent series inductance (ESL) will have to be connected in parallel to the electrolytic capacitor, in order to provide a path for the high-frequency current components and to avoid voltage spikes provoked by the high di/dt on the ESL of the electrolytic capacitor. On the other hand, if a ceramic capacitor is used, the current ripple requirement can be matched by a capacitor of exactly 47μF, 200V, having only half the volume of the electrolytic capacitor, with an ESR of 7mΩ and power losses lower than 0.5W.

losses at higher frequencies. Large air gaps are also recommended, in order to keep the induction and consequently the magnetic losses low. Some studies [9, 75] have shown that the use of low-permeability materials to provide a "distributed air gap" can lead to better performance. A pot core with a shortened center post can also be a good compromise between volume, weight, losses and EMI. In this case, the inductor is essentially an air core inductor, but there is a magnetic shield around it.

Another inductor design concept that is gaining increasing acceptance is the planar design. Planar inductors with sheet-conductor or printed-circuit windings can be very compact, attaining higher power densities. At higher power levels, the planar design can be even more advantageous, because it also provides an improved thermal interface due to the large surfaces available for cooling.

4.2.2 Capacitors

In ACRDCL converters, basically three "types" of capacitors are needed, depending on the location in the circuit where they are used:

- the resonant capacitor;
- the clamp capacitor;
- the DC supply capacitor.

For each of the above types, there are different design requirements, according to the required capacitance range and to the nature of the current that flows through the capacitor. Therefore, a different capacitor technology may be the most appropriate for each location in the circuit. Capacitors are available today in three basic technologies, for use in power electronic circuits up to some hundreds of kilowatts. Currently commercially available technologies are listed below [91]:

4.2.1 Inductors

Air core inductors can be a good choice for some applications, because they produce no core losses and can be lighter than inductors with a magnetic core, but volume and radiated EMI are limiting factors. In addition, at higher power levels, air core inductors can be constructed with smaller dimensions than magnetic core inductors, because the magnetic core may have to be overdimensioned due to thermal problems [75]. EMI radiation can be reduced if a toroidal winding is used, where most of the magnetic flux remains confined in the interior of the winding. The inductance of a toroidal coil with air core can be estimated by

$$L = \mu_0 N^2 \left(g - \sqrt{g^2 - a^2} \right), \tag{4.2}$$

where N is the number of turns, g is the mean radius of the torus and a is the radius of its cross section, as shown in Fig. 4.4.

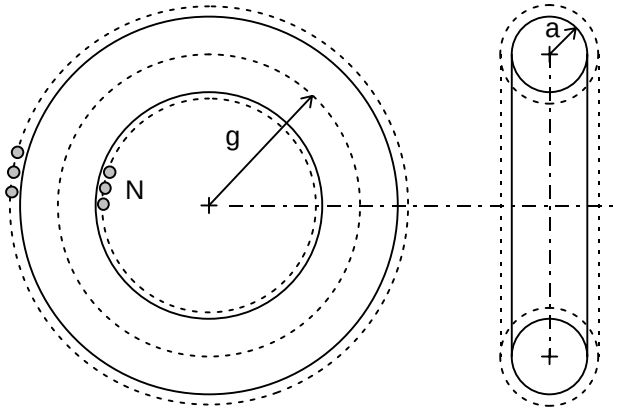


Fig. 4.4: Top view and cross section of toroidal coil.

The winding construction is also very critical with respect to the power losses and the size of resonant inductors designed for operation under high peak values of alternating current and at higher frequencies, because of skin and prox-

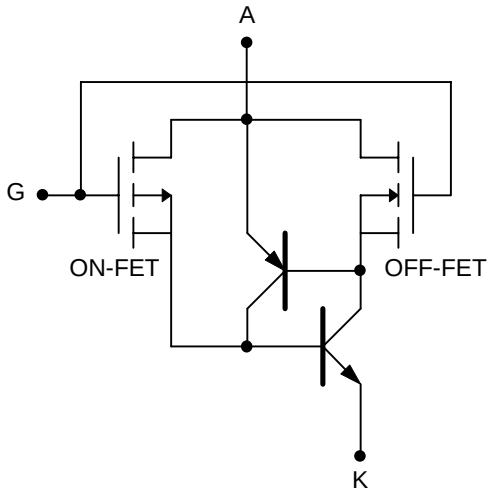


Fig. 4.3: Equivalent circuit of the p-MCT.

The major advantage of MCTs in comparison with IGBTs is the up to 50% lower on-state voltage, which can lead to an up to 50% reduction of the on-state power losses [76]. Typical values of on-state voltages are between 1V and 1.5V for MCTs rated at 1kV, whereas 3rd generation IGBTs of comparable voltage rating exhibit saturation voltages about 2V to 2.5V. On the other hand, MCTs exhibit somewhat higher switching losses than IGBTs in hard-switched mode. Typical values of total switching losses (specific values, normalized to rated current) are under 0.3 mJ/A [77, 98]. Furthermore, the MCT tail current is strongly dependent on the temperature, leading to higher turn-off losses at higher temperatures. Tail current duration is typically about 1µs.

The main drawback of the MCT is its restricted capability to limit and to turn off short-circuit currents. MCTs can conduct much higher currents than IGBTs with the same chip size. However, MCTs and IGBTs have approximately the same maximum turn-off current density, so that there is no chip size advantage if both components are designed to have the same short-circuit ratings. In fact, the MCT turn-off capability depends on the on-state resistance of the off-FET region. When the device is being turned off, the full cathode current flows through the off-FET. If the voltage drop across it is greater than the base-emitter voltage of the npn transistor in the thyristor pair, this latter cannot be

achievable on-state voltage versus total switching energy for a second-generation 600V IGBT is shown in Fig. 4.2.

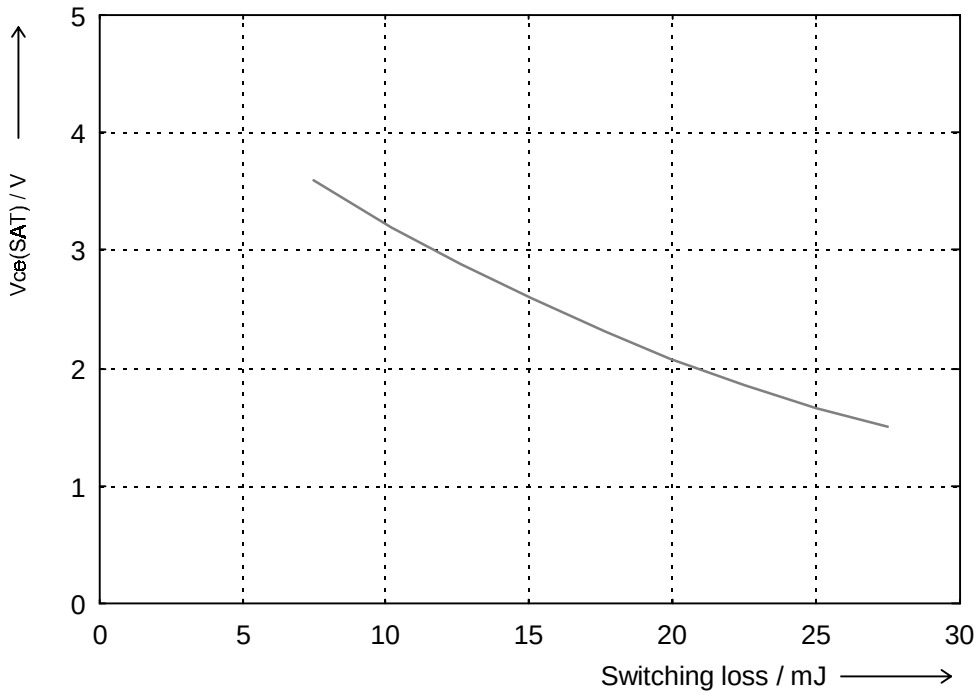


Fig. 4.2: Typical V_{CE}(on) versus switching energy relationship for a 600V IGBT at 1A/mm^2.

Most manufacturers have developed basically two types of second-generation IGBT devices, one optimized for lower on-state voltage drop and consequently lower conduction losses, and another optimized for faster switching speed and lower switching losses. These families have been usually called "low saturation" and "fast switching" respectively. However, further optimization of IGBT chip properties has led to third-generation devices, which exhibit equal or lower conduction losses than second-generation low saturation devices and equal or lower switching losses than second-generation fast switching devices. Typical values of specific switching losses of second- and third-generation devices are shown in Table 4.1 [5, 36, 64].

Another important property related to the unipolar structure of the MOSFET is the very high switching speed. As there is no injection of minority carriers in the drift layer during conduction, there is neither delay nor tail current associated with removal of excess carriers at turn-off. The turn-on process is also very fast, mainly governed by the movement of charge carriers in the depletion layer and in the gate-source stray capacitances. Consequently, switching frequencies up to some hundred kHz can be easily reached in hard-switching mode. If soft-switching is used, the switching frequency can be increased up to some MHz [48]. However, due to the trade-off between current and voltage ratings mentioned above, the use of MOSFETs in electric motor drives is limited to low-voltage and low-power ranges.

4.1.2 IGBT

There are basically two types of IGBT, termed punch-through (PT) and non-punch-through (NPT). The main difference between the two types is the presence of a highly doped n+ buffer layer in the PT IGBT vertical structure, as shown in Fig. 4.1 (b). The purpose of this buffer region is to limit the extent of the depletion layer for blocking voltages higher than a fraction of the device's breakdown voltage. This allows for reduction of the drift region thickness, with attendant reduction of conduction losses. This buffer layer is not present in the NPT IGBT structure, which must therefore have a wider drift region to achieve the same voltage rating. Since this drift region is only lightly doped (low conductivity), conduction losses are expected to be higher than for the PT geometry.

The switching behaviour of the IGBT is also influenced by the type of structure [67,82]. Although the switching mechanisms are basically the same in both structure types, differences in emitter efficiencies and in carrier lifetimes give rise to different magnitudes and durations of the so-called tail current at turn-off. The emitter efficiency influences directly the portioning of the total device current in the two components i_1 and i_2 shown in Fig. 4.1 (b). Component i_1 is a BJT-like current, and its path can be viewed as a pnp bipolar transistor. This

MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) - for low to medium power applications up to some kW. However, high blocking voltage and high current conduction capabilities cannot be attained simultaneously. Low-current devices with voltage ratings up to 1 kV or low-voltage devices with current ratings up to some hundred amperes are commercially available.

IGBT (Insulated Gate Bipolar Transistor) - for medium power applications (<1 MW). By the time of writing of this work, IGBT modules with voltage blocking capabilities up to 3300V and current ratings up to ca. 1 kA have become commercially available [72].

MCT (MOS-Controlled Thyristor) - an emerging device. Current and voltage ratings of MCTs comparable to those of IGBTs are technically possible, but currently available devices have voltage ratings up to 1 kV and current ratings less than 100 A.

As high power applications are beyond the scope of this work, SCRs and GTOs are not dealt with in the following analysis. BJTs are also not considered because of its on-going obsolescence.

MOSFETs, IGBTs and MCTs have high-impedance (isolated) control terminals and consequently lower power consumption at the gate terminal, in comparison to SCRs, GTOs and BJTs. A simplified comparison of the vertical structures of these devices is presented in Fig. 4.1. Their basic features are discussed below [67].

Although the actively-clamped resonant DC link (ACRDCL) converter has been frequently pointed out as the most promising resonant converter topology for medium-power AC drive systems, no other author has published any work on attempting to adapt an ACRDCL converter for application in SR drive systems. Nevertheless, the ACRDCL seems to be a well-suited soft-switching circuit for high power density SR drives, because it has a low number of additional components and the voltage stresses are limited, according to the clamp factor. A possible implementation of ACRDCL SR converter is shown in Fig. 3.16. A detailed analysis of the ACRDCL SR converter is presented in chapter 5.

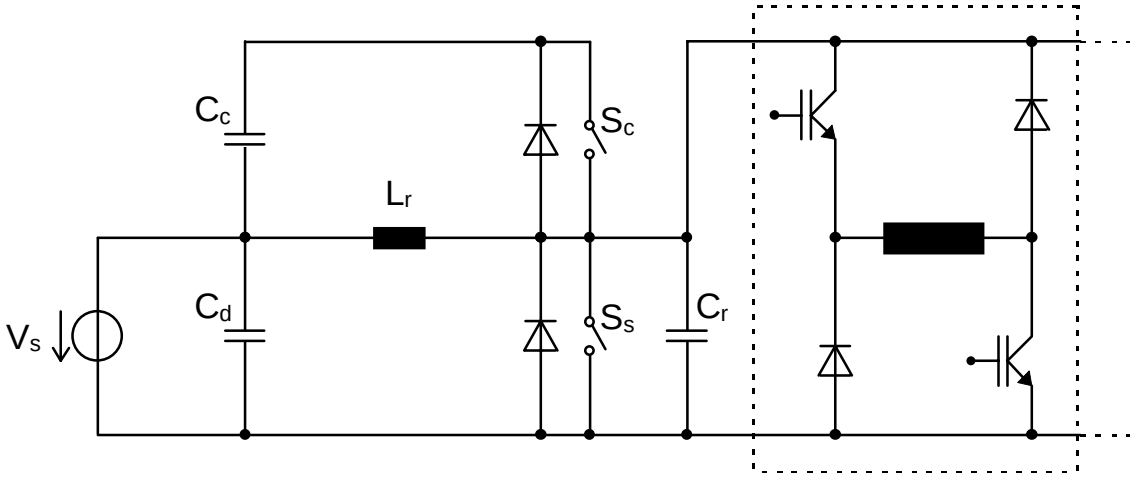


Fig. 3.16: A possible implementation of ACRDCL SR converter.

used only to resonate the DC link voltage to zero, in order to create a zero-voltage switching opportunity for commutation of the main output switches. As switch S must conduct the whole motor current, the conduction losses are expected to be up to ca. 30% higher, for operation in single-pulse mode.

3.2.4 AQRDCL SR converter

In [15], the application of an auxiliary quasi-resonant DC link (AQRDCL) to a SR machine drive is proposed. A schematic diagram of the proposed circuit is shown in Fig. 3.15. In this topology, the switch S_c is kept closed most of the time, connecting the supply voltage V_s to the upper rail of the output section. When the main output switches have to be commutated, a resonant transition is started by triggering the auxiliary zero-current switch S_a into conduction, in order to pre-charge the resonant inductor L_r . Switch S_a is kept closed until the energy is stored in L_r is enough to ensure a full swing of the DC link voltage from V_s to zero. Switch S_c is then turned off under ZVS conditions, and the DC link voltage falls to zero with the waveshape dictated by the resonant tank formed by L_r and C_r . When the DC link voltage passes through zero, the switch S_s is closed, shorting the DC bus and holding its voltage at zero for a brief period, during which the main output switches can be commutated with low switching losses. The duration of this shorting period should be enough for the current in L_r to reverse and to reach a magnitude that will guarantee the full swing of the DC link voltage back to V_s when the switch S_s is turned off. S_s is switched off under ZVS conditions, and the energy stored in L_r will give rise to the resonant oscillation with C_r , that will bring the DC link voltage back to the supply level V_s .

In the circuit of Fig. 3.15, switch S_a must be bi-directional in voltage and current. Furthermore, switch S_c conducts the whole motor current, producing additional conduction losses. If the circuit is operated with tail current overlap, the voltage applied to an offgoing phase during demagnetization will be reduced, because of the DC link resonance required for PWM current control of the next ongoing phase. This shortcoming can be avoided if the upper diodes of

between $-V_s$ and $+V_s$ in order to control the phase current. This requires an interleaving or time-multiplexing of both control loops, and it may be difficult to achieve when the switching frequencies in the two phases are different, due to different current levels. As a result, the turn-off of a phase is strongly coupled to the turn-on of the next phase. In this circuit, the peak voltage stresses can be limited by choosing an appropriate value for ΔV. The peak current stresses are also directly proportional to ΔV and inversely proportional to the characteristic impedance of the resonant tank $Z_r = \sqrt{L_r / C_r}$. The reduced number of switches seems to be the main advantage of this circuit, but they must be rated to more than twice the supply voltage, so the cost savings are low. Furthermore, the control method employed for this converter is very complex and it is expected to exhibit a slower dynamic performance than a directly voltage-fed CRPWM control.

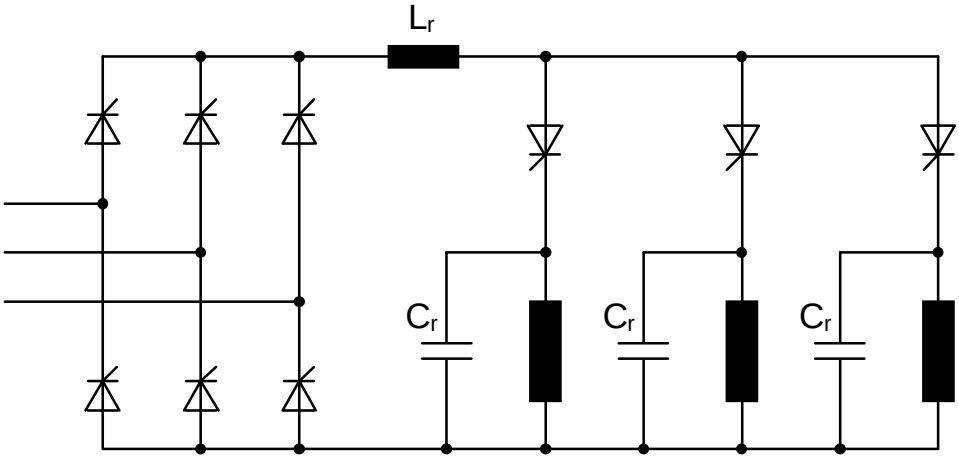
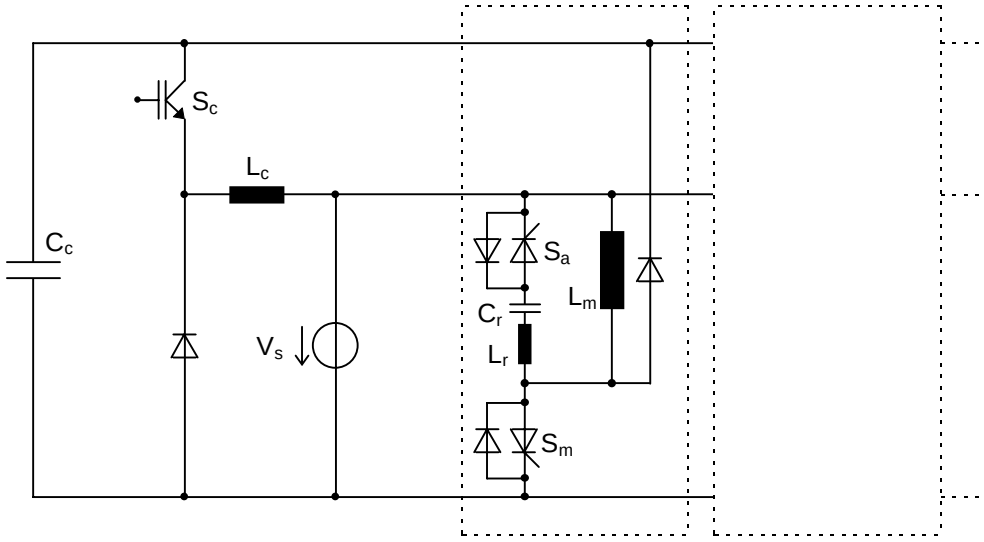


Fig. 3.13: Series-resonant converter for 6/4 SR motor, with three-phase input.

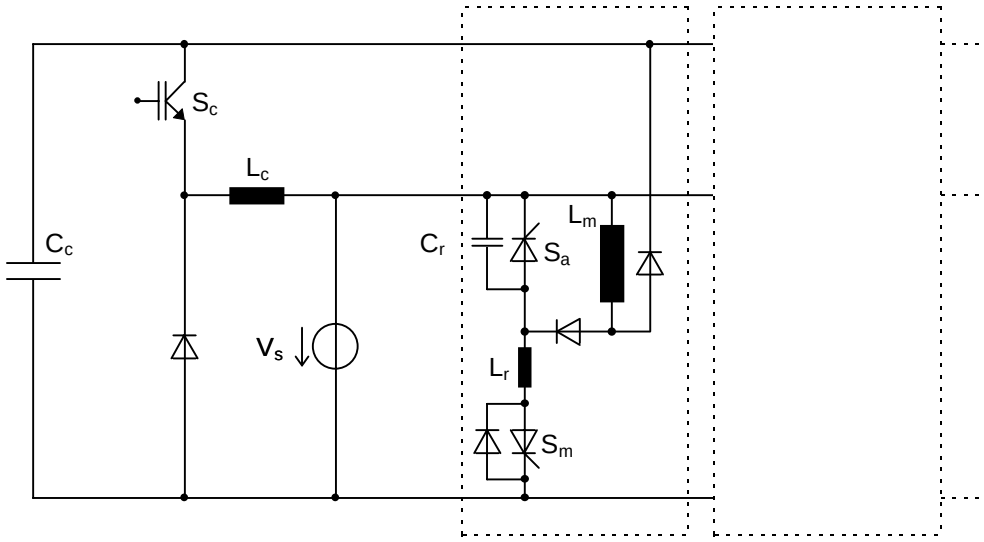
3.2.3 Zero-voltage transition (ZVT) PWM SR converter

In [71], Rim et al. propose the use of a single chopping switch to regulate the DC link voltage of a "Pollock" converter, using true PWM voltage control. The chopping switch (S) is commutated at zero voltage with help from a subcircuit comprising a resonant tank (L_r and C_r) and an auxiliary switch (S_a), as shown

diodes makes the turn-on behaviour of the main switches to be dictated by the reverse recovery characteristics of the C-dump diodes, resulting in no alleviation of turn-on losses. In fact, both circuits are more likely to be classified as force-commutated thyristor converters than as actual soft-switching topologies. The high number of components is the major disadvantage of these circuits.



(a)



(b)

Fig. 3.12: ZCS C-dump converters
(a) circuit proposed by Le-Huy et al. [50],
(b) circuit proposed by Uematsu and Hoft [101].

the output stage can be commutated under zero voltage, with low switching losses. The moments when the DC link oscillation is triggered to create a zero-voltage soft-switching opportunity can be almost freely chosen, provided the resonant frequency is substantially higher than the average switching frequency of the output converter.

The higher degree of freedom in choosing the commutation instants, compared to resonant link converters, enables the utilization of quasi-PWM methods for the output voltage or current control, rendering improved spectral characteristics. However, if simultaneous control of several output phases is required, they cannot be controlled completely independently from each other, because there is only one resonant commutation circuit for all phases. If the output section is composed by half-bridge inverter phase legs, the switch S_s can be removed from the circuit and its function can be performed by the phase legs.

The topologic similarity between the ACRDCL and the AQRDCL should be noticed. If switch S_a is suppressed or kept closed all the time, the AQRDCL can be operated as an ACRDCL in buck mode, with continuously resonating DC link voltage. In this case, the average DC link voltage will be lower than the supply voltage. On the other hand, the ACRDCL circuit shown in Fig. 3.6 is a boost implementation, that allows full utilization of the supply voltage at the output. In the boost ACRDCL, the main power flow occurs through the resonant inductor, which therefore has to be designed for very low power losses. Conversely, in the buck ACRDCL and in the AQRDCL, the main power flow takes place at switch S_c .

3.2 Soft-switching converters for SR drives

The use of soft-switching converters in AC machine drive systems has been already well documented in the literature, with many works having been published, e.g. [8, 19, 21, 22, 39, 44, 45, 73, 89, 96, 97]. On the other hand, just a few reported applications of soft-switching techniques in SR drive systems are

3.1.3.3 Resonant pole converters

The family of resonant pole converters is characterized by the presence of a so-called resonant pole at each leg of the output section. Each resonant pole comprises a resonant inductor and a pair of resonant capacitors. These capacitors are directly connected in parallel with the main output switches, in order to achieve zero-voltage switching. Some resonant pole topologies, like the auxiliary resonant commutated pole (ARCP) converter [13], also include additional switching devices in order to improve the controllability and reduce the current stresses and the conduction losses in the resonant pole. An equivalent circuit for one phase of the ARCP converter is shown in Fig. 3.10. The circuit section enclosed in the dashed box is equal for each output phase. The middle point provided by capacitors C_d is common to all phases.

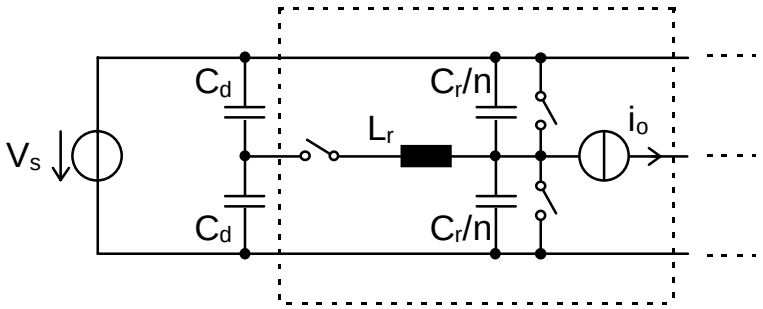


Fig. 3.10: Equivalent circuit for one phase of the ACRP converter.

In contrast to resonant DC link converters, no resonance is produced at the DC link in resonant pole converters. Instead of that, the resonant transitions occur separately at each resonant pole, only when the switches in the output stage need to be commutated. The DC link voltage remains unaffected during the resonant transitions. Therefore, the main switches in the inverter phase legs can be commutated totally independent from each other. This allows a free choice of the commutation instants, thus enabling the employment of "true" PWM control techniques.

104] that the ACRDCL is the most suitable soft-switching converter topology for medium-power AC drive applications.

Series resonant DC link (SRDCL) converter

The SRDCL converter [68] is obtained by adding a resonant tank to a current-regulated DC link converter. An example of three-phase AC to three-phase AC SRDCL converter is shown in Fig. 3.8. The topology is very similar to the SRACL converter, but in this circuit, the switches do not need to conduct in both directions as in the SRACL. However, they must be capable of blocking direct and reverse voltage. The DC link current of the SRDCL converter can be described as the sum of a high-frequency AC component (as in the SRACL), produced by the resonant tank, plus a DC bias provided by the smoothing inductor L_d . To provide this DC offset, L_d must be much larger than the resonant inductor L_r and its current must be regulated by controlling the output voltage of the source-side converter. The input and output switches are commutated with low switching losses, when the resonant DC link current crosses zero, hence under ZCS conditions.

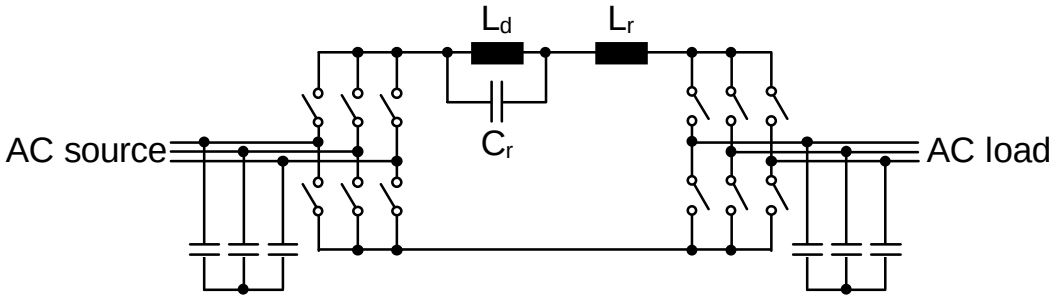


Fig. 3.8: SRDCL converter.

The operation of the SRDCL converter is in many aspects dual to the operation of the PRDCL converter. The duality can be better understood with help of the equivalent circuit shown in Fig. 3.9. The current source I_d is used to represent the current in the smoothing reactance L_d (Fig. 3.8), because the current in L_d does not change appreciably during one resonant cycle. Comparing this circuit

The modeling assumptions mentioned above for the PRDCL converter are also valid for the ACRDCL converter. Circuit operation of the ACRDCL is also very similar to that of the PRDCL. An operating cycle starts when switch S_s is switched on. S_s is kept closed until enough energy is stored in L_r to ensure that a full resonant cycle will be completed. S_s is then released, the current through L_r is pumped into the resonant capacitor C_r, and the voltage v_{Cr} across C_r starts to rise towards its natural peak. When v_{Cr} reaches a value equal to $(V_s + v_{Cc})$, the clamping process starts. The clamp diode across S_c begins to conduct, diverting the current from the resonant capacitor into the clamp capacitor. While the clamp diode is conducting, switch S_c can be turned on, under zero voltage conditions and with low switching losses. S_c is kept on until the current in the clamp capacitor reverses and reaches a preset current level I_c , at which S_c is turned off. Immediately after turn-off of S_c , the inverted current which was flowing in the clamping circuit will be transferred back to C_r , causing the DC link voltage to oscillate toward zero. When v_{Cr} reaches zero, the anti-parallel diode of S_s will conduct and then a new cycle can be initiated. The resulting DC link voltage waveform is qualitatively shown in Fig. 3.7.

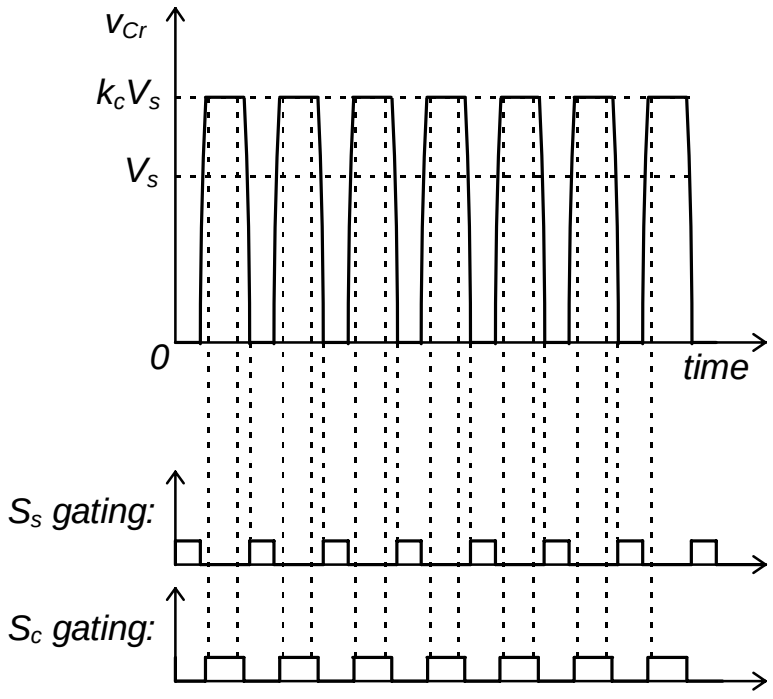


Fig. 3.7: DC link voltage of the ACRDCL converter.

resonant DC link and ensure that the subsequent oscillation will bring the DC link voltage back to zero. Switch S_s can now be released and, after the DC link voltage has performed a complete oscillation and returned to zero, S_s is turned on again in order to give continuity to the process. The resulting DC link voltage waveform is qualitatively shown in Fig. 3.5. While S_s is closed, the main output switches can be commutated under zero-voltage switching conditions, distributing the DC link voltage pulses among the output phases. When S_s is opened, the presence of the resonant capacitor C_r in parallel to it ensures that its own turn-off also occurs under zero-voltage switching conditions. The excess energy stored in L_r while S_s is closed will generate a peak DC link voltage higher than twice the supply voltage. When the DC link voltage oscillates downwards, it will tend to become negative, but will be clamped at zero volts by the anti-parallel diode of S_s . While the diode is conducting, S_s can be turned on without switching losses, also under zero-voltage switching conditions.

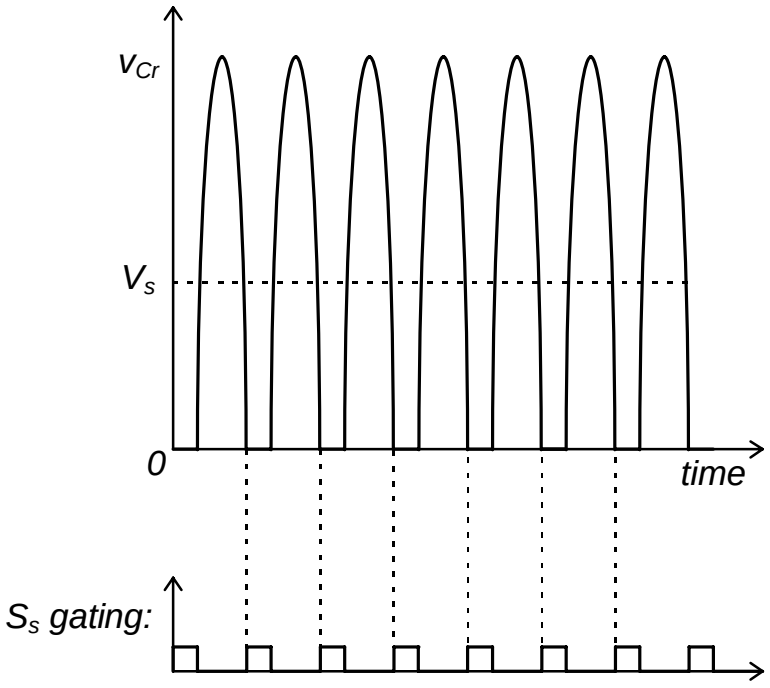


Fig. 3.5: DC link voltage of the PRDCL converter.

3.1.3.1 Resonant AC link converters

In resonant AC link converters, the resonant tank in the AC link produces a high-frequency alternating voltage (PRACL) or a high-frequency alternating current (SRACL), in combination with proper operation of the input converter. The switches of both the source-side and the load-side converters are turned on and off when the voltage (PRACL) or the current (SRACL) in the DC link passes through zero, minimizing the switching losses. The switching patterns of the input and output converters should provide the distribution of packets of integral half-cycles of the high-frequency AC link voltage or current among the phases of the input and output converters. The pulse distributions at the input and at the output should exhibit as fundamental components the desired low-frequency voltages or currents. Due to the finite time that must be held between switch commutations (the period of the zero-crossings in the high-frequency AC link), input and output control can only be achieved by discrete-time control methods, like pulse density modulation methods [89]. Conventional PWM control is not applicable.

In a PRACL drive system, the source-side converter must be current-sourced and the output of the converter at the load-side must exhibit a current-sink behaviour. PRACL and SRACL drive systems are dual to each other, so that the source-side converter in a SRACL driver system must be voltage-sourced and the output of the load-side converter must determine the voltage. For motor loads, capacitors must be connected in parallel to provide this behaviour. Since the input and the output as well as the AC link quantities are alternating, the resonant AC link converter requires that all the switches at the input and at the output be bi-directional in current conducting and voltage blocking capability. For each bi-directional switch, two controllable power semiconductor devices must be used, rendering a high number of costly active components. For this reason and due to the complex control, this type of converter is considered uneconomical for general-purpose industrial drive applications in the medium-power range.

modifications in the resonant-switch circuits allow the use of pulse-width modulated control [2]. This type of converter, however, has limited applicability in medium- to high-power electric motor drive systems, due to the higher current stress and associated conduction losses in the resonant switch in ZCS mode, as well as the higher voltage stress in ZVS mode. The main application area for this kind of converter is the field of switch-mode power supplies.

3.1.3 Soft-switching converters for motor drive applications

In electric motor drive applications, soft-switching converters are usually classified in three categories, namely *resonant pole* converters, *resonant DC link* converters and *resonant AC link* converters [21]. Detailed descriptions and comparative analysis of these converter types can be found in [22, 89] and will be summarized here. Table 3.1 shows in condensed form the main basic topologies of the above mentioned converter families. There exist many circuit variations in each family, but the placement of the reactive components which produce the resonant transition is what distinguishes a family from the others, and this has been highlighted in Table 3.1. Circuit variations and main characteristics of these converters are discussed further below. The output section of the converters in Table 3.1 is shown in a dashed box for one AC phase only, but in an actual application there would be a number of such sections, depending on the number of machine phases.

Electric motor windings are highly inductive and its input current changes slowly in comparison to converter switching times. Hence, they can be modeled as current sinks. For this reason, it is more convenient to feed them with voltage-source converters (VSC), except for very high power levels above some megawatts, where current-source converters (CSC) may be more economic. The technological reason for that is the better suitability of thyristors as power switches for very high power levels. However, in this case load commutation is used and therefore the switching is done at a very low frequency. In this situation, thyristor CSCs are more attractive, because they are much simpler, and therefore more rugged and reliable at such power levels, than thyris-

(Fig. 3.2 (a)), if a positive voltage step is applied to the load by closing switches S_1 and S_4 , the load current undergoes a free oscillation. As the current inverts, the corresponding anti-parallel diodes will conduct and the switches S_1 and S_4 can be opened without switching losses. Switches S_2 and S_3 can now be closed, inverting the voltage applied to the load and forcing its current to oscillate continuously, in a sustained resonance. The power flow to the load is controlled by the resonant tank impedance, which in turn depends on the switching frequency. This type of circuit is not very suitable for use with dynamic loads like electrical machines, in particular with SRMs, which exhibit inductances that change with position and current in a wide range, in a highly nonlinear manner. The main application field for this type of converter is induction heating.

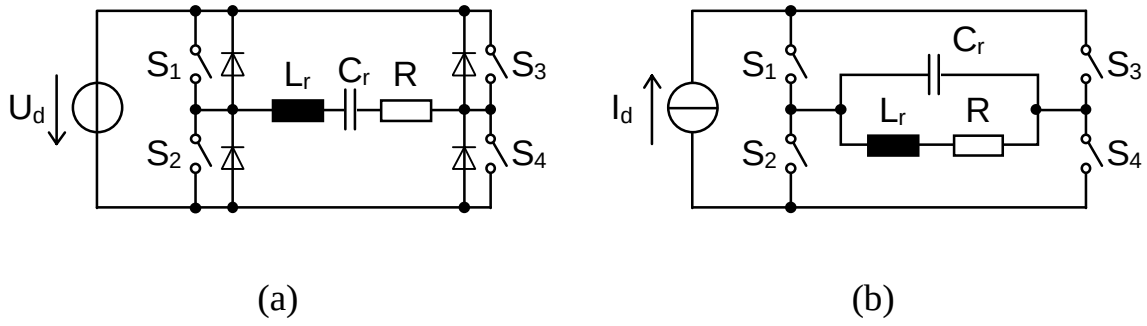


Fig. 3.2: Series-resonant (a) and parallel-resonant (b) converters.

3.1.2 Resonant-switch converters

A resonant switch is obtained by connecting resonant LC elements to a power semiconductor switch. Some basic resonant switch configurations are shown in Fig. 3.3, but an extensive analysis of many circuit families of this kind can be found in [48]. The operating mode of a resonant-switch converter depends on the placement of the LC elements with respect to the power semiconductor element.

methods of achieving switching stress alleviation can be thought of as a continuous evolution in type of response, as represented in Fig. 3.1 [104].

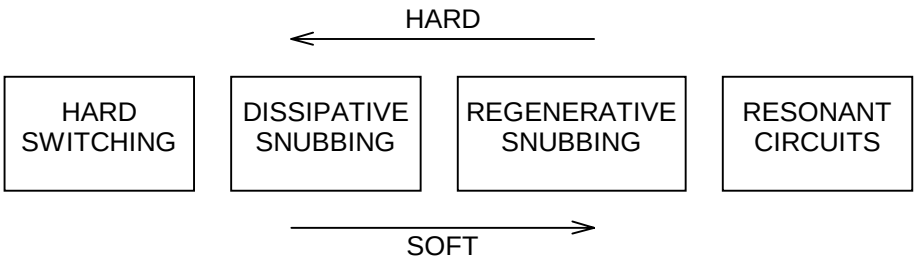


Fig. 3.1: From hard-switching to soft-switching.

3.1 Classification of soft-switching converters

The term soft-switching is very broad and can be globally used to designate many different concepts and topologies [67]. Classification of soft-switched converters is not uniform among distinct authors. Many authors prefer the general designation "resonant converters", but it sometimes leads to misunderstandings. Many soft-switching converters are not truly resonant. In several topologies, resonance (in fact only part of a free LC oscillation) is limited to the switching transitions, which has led to the terminology "resonant transition converters". In other soft-switching converters, the link voltage or the link current is turned to zero during short periods of time, creating opportunities for the main switches to be turned on or off . Previously, soft-switching converters used to be classified as *resonant* and *quasi-resonant* only. As soft-switching technology evolved, many new topologies were proposed, which did not fully complied to those categories. In [67] the following classification of soft-switching converters is proposed:

- Load-resonant converters
  - Voltage-source series-resonant converters:
    Series-loaded resonant (SLR) converters;
    Parallel-loaded resonant (PLR) converters;
    Hybrid-resonant converters.

phase currents does not reverse in the phase windings, the mean value of the DC link current becomes negative during braking, due to the power reversal. Therefore, the DC supply must be able to absorb the recovered braking energy.

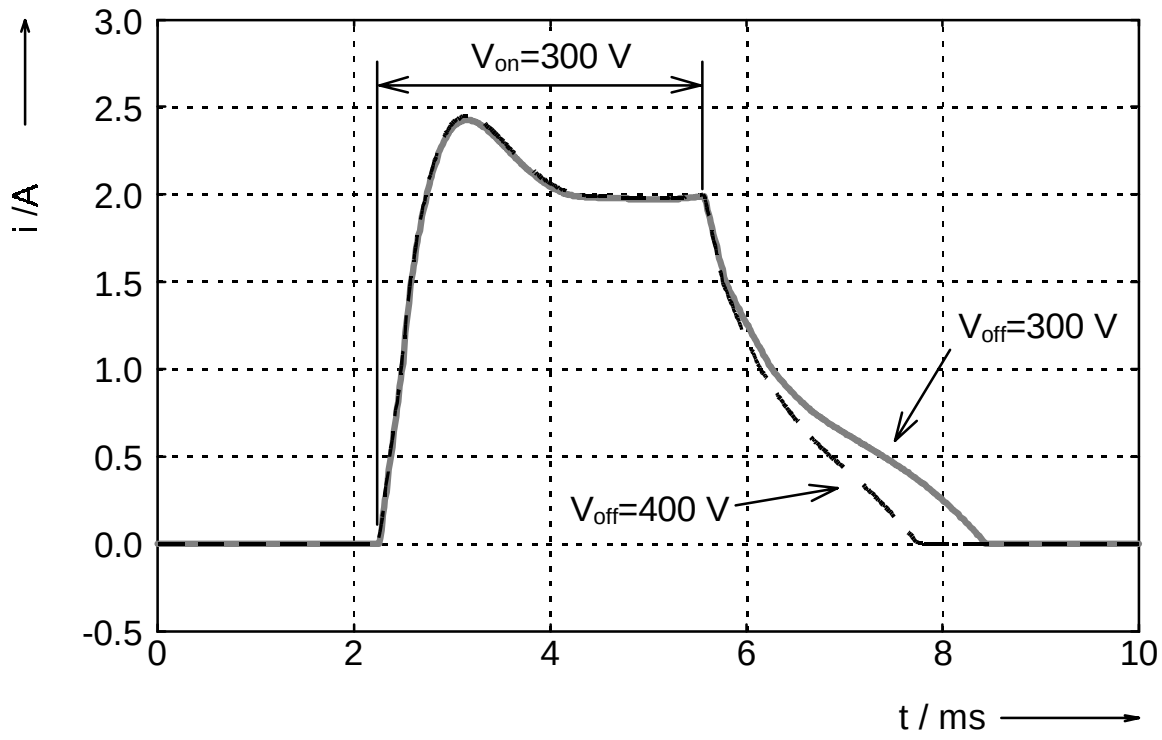
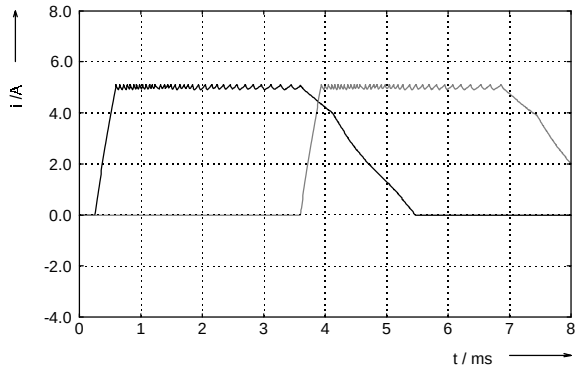


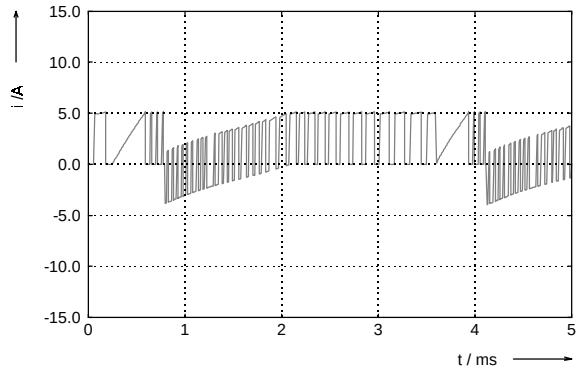
Fig. 2.16: Current pulses for different values of demagnetizing voltage.

2.4.2 Regenerative Braking and Reversion

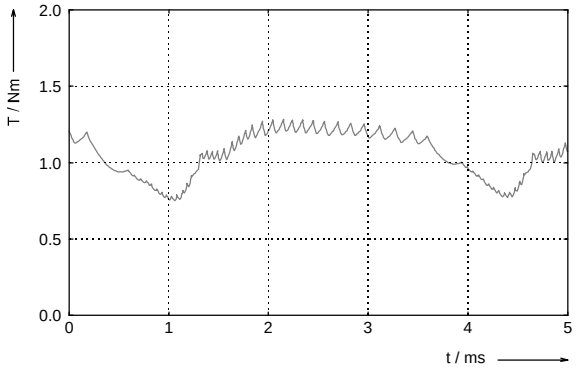
The operation of the SRM in regenerative braking mode can be achieved by merely shifting the current pulses for each phase into the decreasing inductance region, where braking torque is produced (cf. Fig. 2.3). The polarity of the phase currents does not need to be reversed, because it doesn't have any influence upon the output torque. However, the region where the inductance decreases depends on the sense of rotation. So, the motoring region for forward rotation is the braking region for reverse rotation and vice versa. The commutation signals for one phase at motoring and braking in both forward and reverse rotation are shown in Fig. 2.17. The braking commutation signals may already begin at the end of the motoring torque production region, in order to provide more time for the phase current to build up. The current build-up is somewhat slow due to the high inductance near the aligned position.



(a)



(b)



(c)

Fig. 2.14: Alternative commutation method combining free-wheeling and dwell overlap (simulation results for 300V supply and 1500 rpm). (a) phase currents; (b) DC link current; (c) output torque.

Fig. 2.13 (c) and Fig. 2.14 (c)), with essentially the same current stress in the DC link. Wu and Pollock [106] have also reported that a free-wheeling period before the final turn-off of the phase current can help to reduce acoustic noise. The waveforms shown in figures Fig. 2.13 and Fig. 2.14 have been obtained from digital simulations, which are thoroughly discussed in section 5.1.

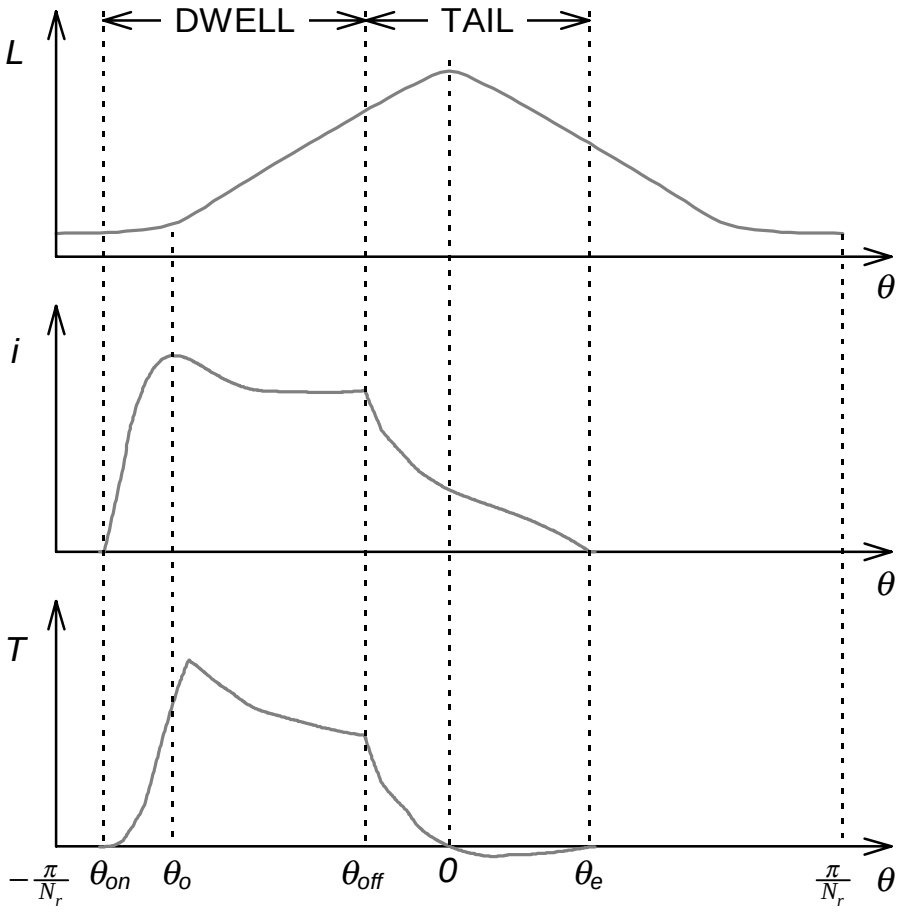


Fig. 2.12: Typical single-pulse waveforms with commutation angle definitions:
(a) inductance variation;
(b) current variation;
(c) torque variation.

For the SR machine to operate with high efficiency, the commutation (turn-off) angle should be close to the aligned position in order to maximize the motoring torque production. It is also desirable to have a short tail period after commutation. The duration of the tail period depends on the difference between the voltage applied to a phase winding at turn-off and its counter-emf. Immediately after the phase current is turned off, the applied voltage reverses, but the counter-emf maintains its polarity. A large voltage difference is then available at the beginning of the commutation, causing a sharp decrease of the phase cur-

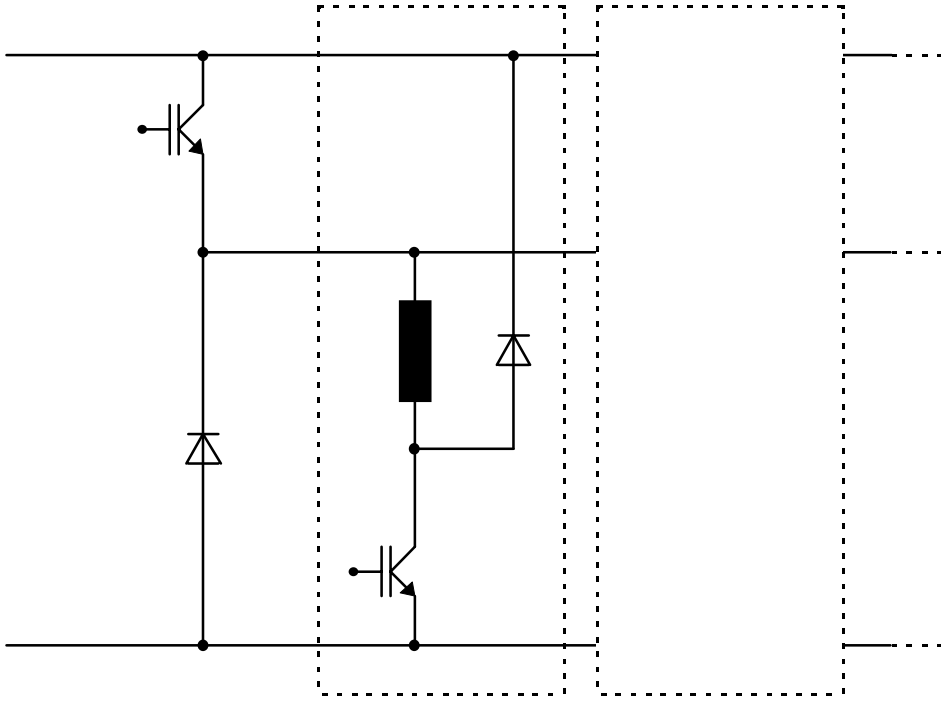


Fig. 2.11: "Miller" converter.

Among the circuit topologies shown above, there is no one which is universally better than the others for all applications. Depending on the motor power and voltage ratings, constructive characteristics and load requirements, one topology can be more cost-effective than the others for a specific application. For example, in low-voltage, low-power applications for mass production, the "Miller" circuit may be a good choice [69]. In applications where high reliability is required, the "classic" topology is clearly the best choice, because the totally independent circuits for each phase provide a high degree of fault-tolerance. Also, for medium power general-purpose industrial drive systems using three-phase motors supplied from the rectified 400V AC mains, it seems to be hardly justifiable to choose a circuit topology other than the "classic" converter, because it causes lower voltage stresses on the power semiconductors, DC link capacitor, machine windings etc. For further reading, a good discussion about converter selection and a detailed comparative evaluation of some SRM converter topologies can be found in [102].

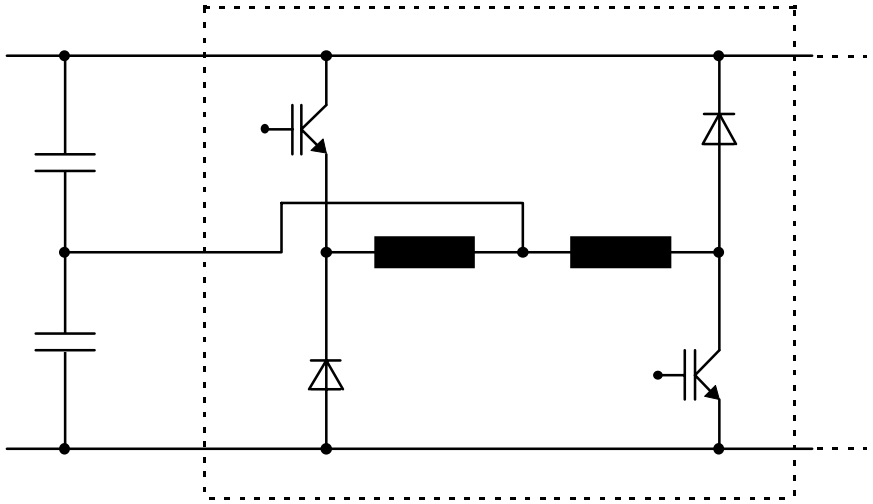


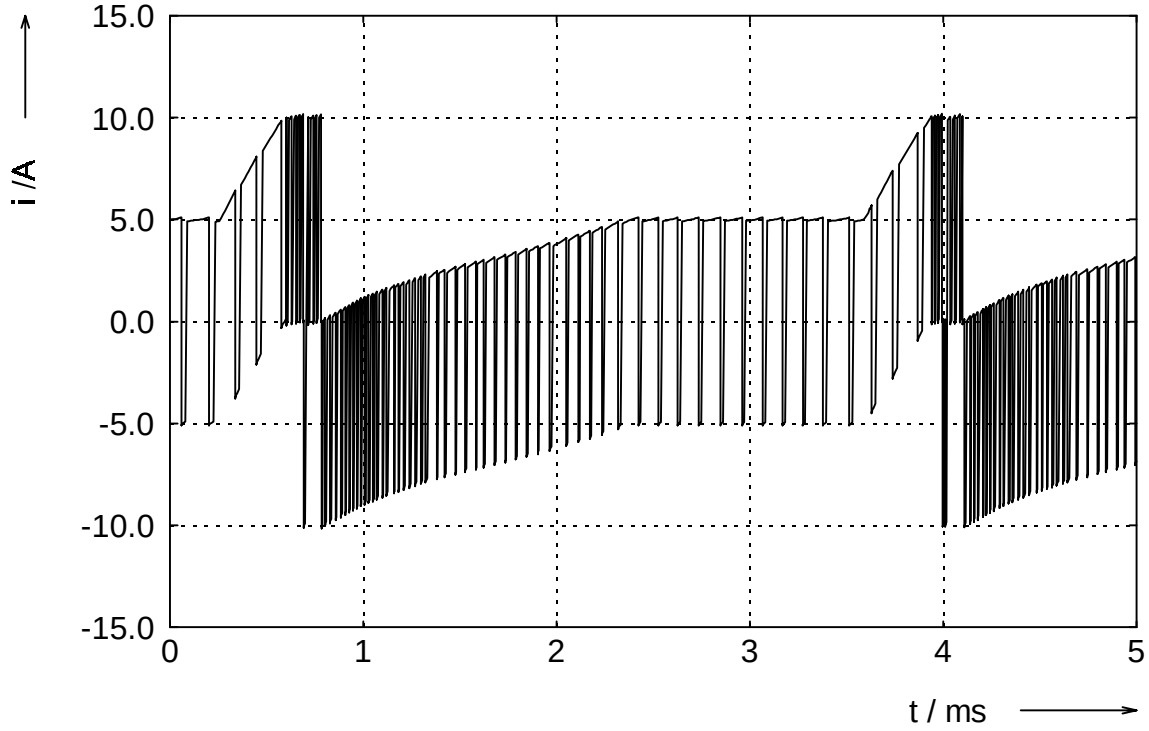
Fig. 2.9: Section of the "Oulton" converter.

In contrast to the topologies shown above, which have independent switches for each phase, there exist many other topologies where the power semiconductor switches are shared among one or more phases. For example, Pollock and Williams [74] have proposed a family of converters which use n_U upper switches and n_L lower switches and are capable of driving SR motors with up to $n_U \cdot n_L$ phase windings. Their topology is based on the building block shown in Fig. 2.10. These converters may be a good choice for SRMs with a high number of phases, because in this case it is possible to use less than one switch per phase. For example, it is shown in [74] how a converter with only six switches can be used to drive a nine-phase motor. However, this type of converter suffers from restricted current control if used with a three-phase motor. The reason is that two adjacent phase windings must share one switch in the three-phase Pollock converter. Therefore, when one of the two adjacent phases is being demagnetized, with both the upper and the lower switches turned off, then the other phase cannot be turned on, because the shared switch is off.

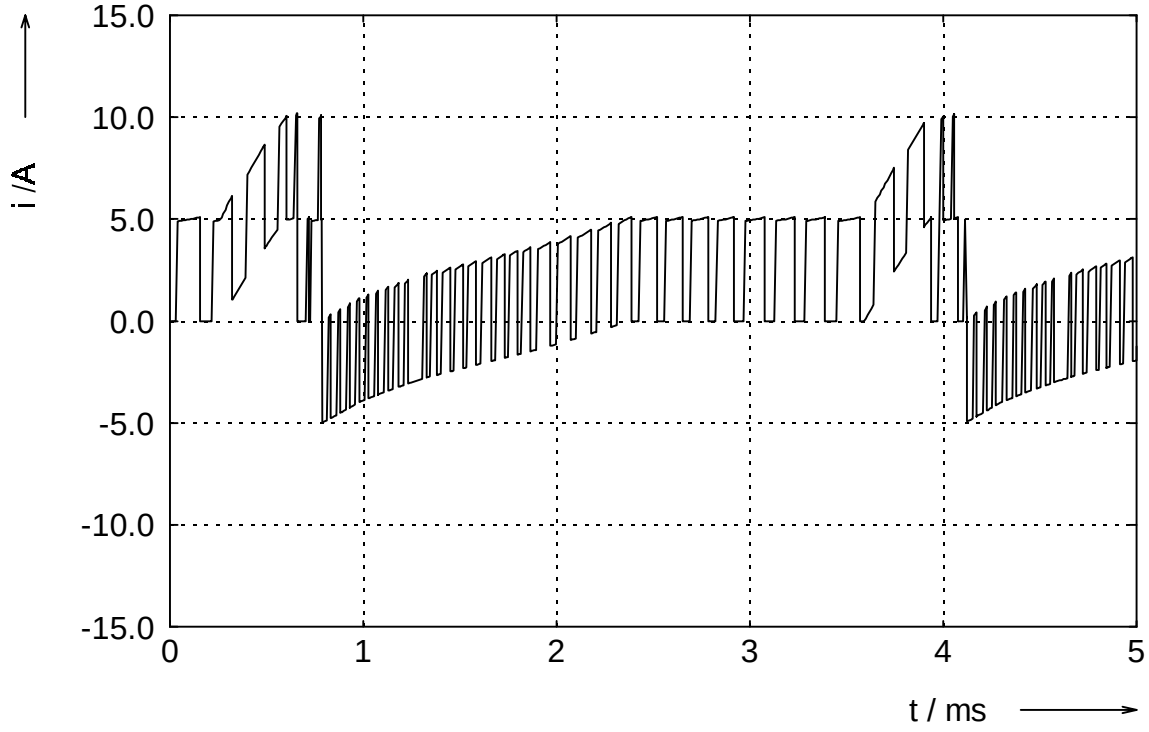
The above configuration has also a high degree of independence between phases, like the asymmetric bridge converter, but it exhibits the following disadvantages:

- inherent hard-chopped operation, because there is no zero-voltage freewheeling path for the phase current;
- additional voltage spikes in excess of twice the supply voltage, due to imperfect coupling between the windings of a phase.
- an inefficient use of machine copper, because two approximately equal windings must be mounted around each pole, but one of them conducts current only for a short time, during the demagnetization period;

Another family of SRM converters with independent circuits for each phase is the one exemplified by the C-dump converter, shown in Fig. 2.8. There are many topological variations which are very similar to the C-dump converter concerning the operating principle, like the "buck-boost" converter, the "sood" converter and the "energy-efficient" C-dump converter [63]. The main idea of this range of converters is to create a second voltage bus (capacitance C_c in Fig. 2.8) for reverse polarization of the phase windings during demagnetization at turn-off. The voltage level at the second bus is regulated by a chopper (switch S_c and inductance L_c in Fig. 2.8). With exception of the converter in [63], the converters of this family have the disadvantage of allowing only hard-chopped operation. The voltage rating of the main switches is about twice the supply voltage, because the voltage at the second rail is usually regulated to this value, in order to provide a demagnetizing voltage equal to the supply voltage. Hence, these converters also have roughly the same total VA rating as the classic topology.



(a)



(b)

Fig. 2.6: DC link current for (a) hard- and (b) soft-chopping (simulation results).

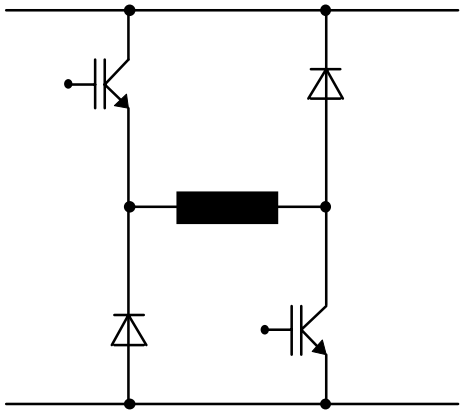


Fig. 2.5: Building block of the "classic" SR converter topology.

The circuit shown in Fig. 2.5 can operate in several different manners. For *single-pulse* operation, the switches are not chopped while the pertaining phase winding is conducting. They are switched on and off only once, respectively at the beginning and at the end of the conducting period. Alternatively, the switches are chopped if the converter operates in the fixed-frequency pulse width modulated (PWM) mode or in the current-regulated pulse width modulated (CRPWM) mode. For chopped operation, the power switches of the classic converter can be operated in one of the two following modes:

hard chopping - both switches of a phase are pulsed in order to achieve current control. The phase current is returned to the DC link whenever the switches are open, i.e. there is no free-wheeling of the phase current. This causes a higher current stress on the DC link capacitor. If the switches are operated with voltage PWM in a fixed-frequency, the phase current ripple will be higher than it would be with freewheeling. For current-regulated PWM operation, the switching frequency will be higher. However, this operating mode is necessary for active braking or if the machine operates as a generator.

soft chopping - only one of the two switches of a phase is pulsed to perform current regulation. The other one remains closed all the time while the phase is

mechanical load has a moment of inertia J_L , a total viscous friction coefficient *B*, and demands a load torque T_L :

$$(J_{SRM} + J_L)\frac{d^2\theta}{dt^2} = T_e - T_L - B\frac{d\theta}{dt}. \tag{2.11}$$

2.3 SR Converter Topologies and Ratings

Several converter topologies have already been proposed for SR drives, each having its own advantages and drawbacks. Despite of the greater flexibility in choosing a converter for a certain application, this abundance of different configurations represents a difficulty for SR drives in gaining market share. In opposition to AC drives, where there are few converter topologies, for SR drives there are many options. Furthermore, because the motor windings must be connected in series with the power semiconductor switches, industry-standard power semiconductor modules cannot be optimally used. The modules have been developed for AC drives, and there are no similar standard modules for SR drive circuits yet. This is a considerable disadvantage, because the converter assembly becomes more expensive and less compact than converters for AC drives, i.e. the maximum attainable converter power density is restricted. Here, the author believes that when the problems are solved and a circuit is settled for SRM drives, possibly a compact power device will be developed. The studies being developed nowadays are important to show the real feasibility of this drive.

Regardless of the topology, a converter for SR drive systems should ideally exhibit the following characteristics:

- it must supply unipolar current pulses to each phase, synchronized to the instantaneous rotor position;
- it should be able to control the magnitudes and possibly also the waveforms of the phase currents;

The total energy $W=W_1+W_2$ supplied to the machine during one phase stroke can be expressed in terms of the maximum flux-linkage and of the maximum current by the expression:

$$W = k \cdot \psi_{max} \cdot i_{max} . \tag{2.5}$$

The factor k is a characteristic of the machine and depends on constructive and operative parameters. Values of k about 0.7 are typical.

Combining equations (2.4) and (2.5), the total energy W can thus be expressed as:

$$W = k \frac{V_s \delta}{\omega} i_{max} . \tag{2.6}$$

The amount of energy converted into mechanical form (W_1) can also be expressed as a fraction of the total energy W as in:

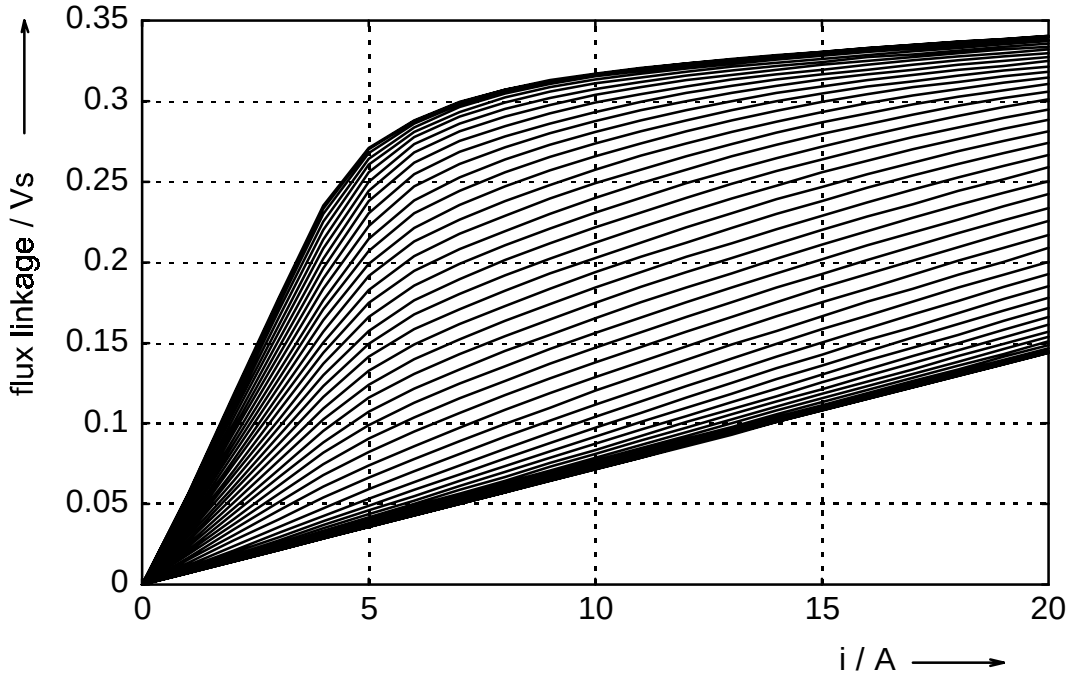
$$W_1 = \varepsilon W = \varepsilon k \frac{V_s \delta}{\omega} i_{max} . \tag{2.7}$$

The factor ε is defined as the energy conversion ratio of the SRM, i.e. the ratio between the energy that is effectively converted into mechanical power and the total electrical energy absorbed by the SRM from the source. It is a concept analogous to the power factor of AC machines. The magnitude of ε depends strongly on operative parameters such as speed and turn-off angle, but is also related to constructive parameters like machine geometry and number of turns of the phase windings. Well-designed SRMs will exhibit values of ε in excess of 60%. The peak per-phase VA requirement of the SRM can be estimated from equation (2.7) and is found to be:

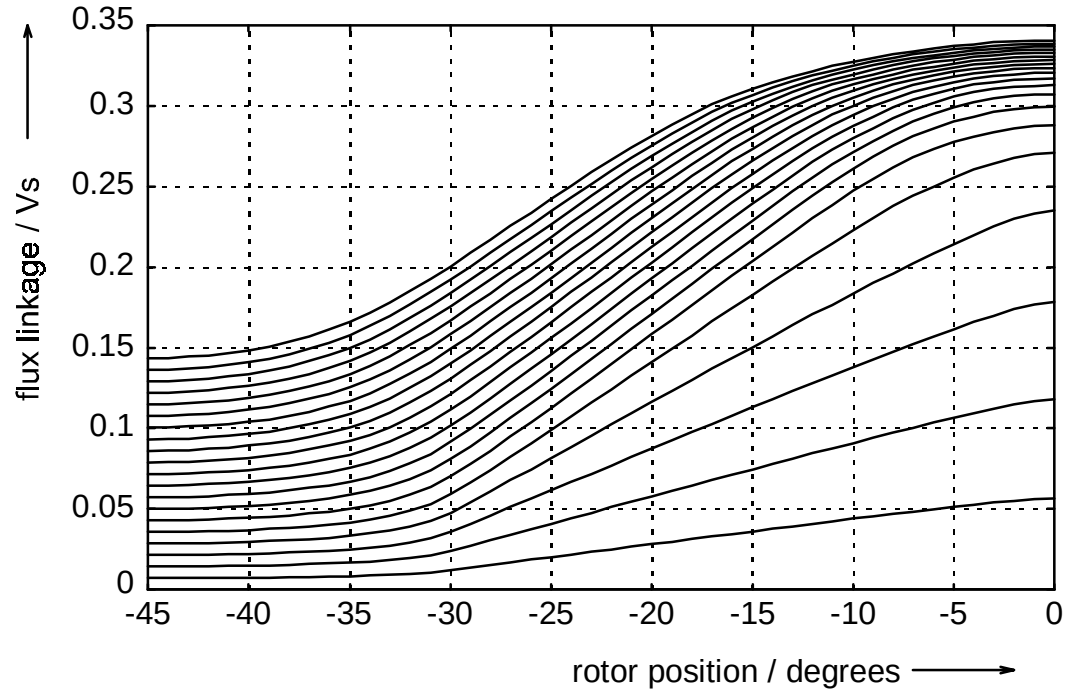
The amount of energy converted by the machine from electrical form into mechanical form at each phase stroke can be derived from the area enclosed by the trajectory of the instantaneous operating point in the flux linkage vs. current diagram. This trajectory is also termed energy-conversion loop. An example of an ideal energy-conversion loop is shown in Fig. 2.4. The loop is limited at the bottom by the magnetization curve for the unaligned position and at the top by the magnetization curve for the aligned position (area W_1). For the phase current and flux of a SRM to follow this trajectory while the rotor is running, the driving circuit would ideally have to be able to:

- make the current rise from zero up to its rated value virtually instantaneously, before the rotor moves away from the unaligned position;
- keep the current constant as the rotor moves from the unaligned to the aligned position;
- make the current fall from its rated value to zero also instantaneously, before the rotor moves away from the aligned position.

The total amount of energy supplied by the converter to the machine during one phase stroke is given by the total area W_1+W_2 in Fig. 2.4. However, after the phase current is turned off at point *b*, the energy given by area W_2 is returned to the source.



(a)



(b)

Fig. 2.2: Typical magnetization curves of a SRM: (a) flux linkage vs. current for different rotor positions between -45° (lower trace) and 0° (upper trace), at 1° intervals; (b) flux linkage vs. rotor position for different current magnitudes between 0A(lower trace) and 20A (upper trace), at 1A intervals.

in equation (2.2). According to [55], under conservative assumptions, the ratio P/D_i^2L for the SRM is about 12% higher than that of a typical squirrel cage induction machine of same speed. This figure was derived under the assumption that the efficiencies of the two machines are comparable and that the SRM operates with a peak air gap flux density (B_g^{SRM} = 1.4 T) twice as high as the peak air gap flux density (B_g^{IM} = 0.7 T) of the induction machine. However, the SRM can be operated at even higher air gap flux densities as has already been mentioned above. Furthermore, to assume that both machines have the same efficiency is equivalent to neglect the copper losses in the rotor of the induction machine. If the total copper losses of both machines were to be equated, the stator current density of the SRM could be increased by at least 20% with respect to the IM, thus yielding a power density about 63% higher than the induction machine. Miller [60] quotes values of 62% for the torque per unit rotor volume and 31% for the torque per unit stator volume, comparatively higher than those of an induction motor. However, only a few works on experimental evaluation of power-density for SRMs have been published. Some of them [29, 66] do not confirm the above predictions, but in [46] a comparison between a SRM and an induction motor has shown that the SRM exhibits a specific output per unit core volume about 40% higher than the induction motor. The compared motors had the same rated power (10 kW), the same frame, the same insulation class, and the following characteristics:

	IM	*SRM*
rated speed (rpm):	1800	1800
torque per core volume (kNm/m^3):	6.75	9.5
output power per core volume (MW/m^3):	1.27	1.79
drive efficiency at rated speed:	81%	86%

Due to saliency and saturation, the SRM has highly non-linear static and dynamic characteristics. It is interesting to notice that these non-linearities are responsible for most advantages as well as for most disadvantages of the motor, so it is difficult to compensate its deficiencies without degrading its performance. Some of the most serious shortcomings of the SRM are the torque pulsa-

the marked phase. This is the position of minimum reluctance or maximum inductance for that phase. If the rotor is displaced by 45° in any direction, then the unaligned position is reached, where the reluctance is at a maximum.

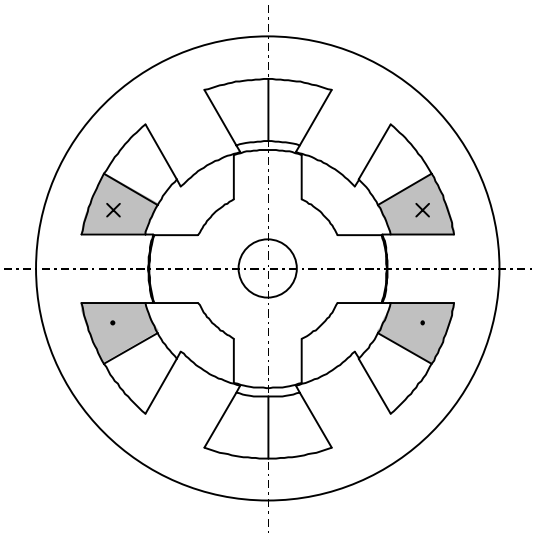


Fig. 2.1: Cross section of a 6/4 SRM.

If one phase of the SRM is energized while the others are not conducting, the rotor will move to the nearest aligned position with respect to that phase. To keep the rotor running, this phase should be then turned off and the next phase should be turned on. If this commutation process is repeated periodically, the rotor will move stepwise, like a stepping motor. This mode of operation offers a very poor stability and very limited output torque capability. The operation is greatly improved if the commutation is synchronized with the rotor position. Rotor position information obtained from a position sensor or through some estimation method is fed back to the motor controller, and each phase receives a current pulse immediately before the rotor reaches the aligned position. This process is described with more detail in section 2.4.1. With the phase currents controlled this way, the rotor turns continuously, but the produced torque is not essentially smooth. Smooth torque can be achieved by appropriate shaping of the current pulses, but this mode of operation requires a very complex control system [92].

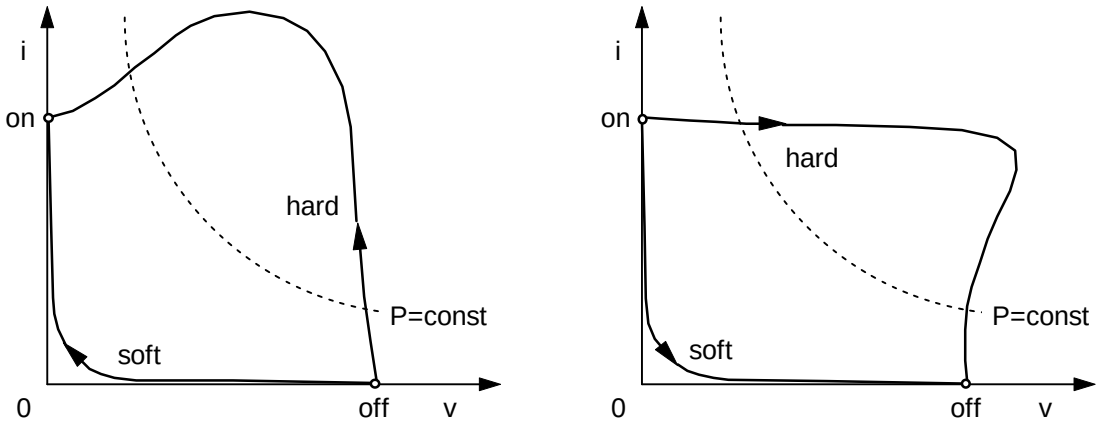
Technological considerations about the various components of the proposed system are presented in chapter 4.

In chapter 5, a drive system with the proposed characteristics is studied. Computer simulation is used as a design tool, because the model of this drive system is too complex for designing a control system analytically. The simulated system is then implemented and the experimental results are discussed to assess the validity of the proposed ideas.

The simulation model developed and validated in chapter 5 is then used in a comparative evaluation between medium-power hard- and soft-switched converter. The discussion of these comparison results is presented in chapter 6.

Finally, a summary of the main results of this work and some suggestions for further developments are given in chapter 7.

fall, the instantaneous voltage and current follow a trajectory that encloses a large area. At turn-off, a similar trajectory is followed. Both trajectories yield a high $\int vi\,dt$ (i.e. switching loss), since voltage and current are simultaneously high most of the time. With soft-switching, conversely, the switching trajectories are very close to the axes and the switching losses are thus lower.



(a) turn-on *(b) turn-off*

Fig. 1.1: Switching loci for hard- and soft-switching.

The amount of energy dissipated during the switching process depends also on the switching times. As semiconductor technology advances, new power semiconductor switches are developed which are faster and thus have lower switching losses. This has allowed a progressive increase in the switching frequency of power converters for electric drives in the last years and because of this, there has been little need for using soft-switching in general-purpose electric drives. Therefore, soft switched converters have not obtained wide industrial acceptance, and this tendency is expected to be maintained in the near future.

However, soft switching converters can still find use in specialized areas where a high power density stands in the foreground, like aerospace applications and small vehicle traction. Some of these areas also require some other properties

- **good thermal behaviour**, due to low heat production and absence of temperature-sensitive structures in the rotor (this can also contribute to increase the power density);
- **lower costs,** due to lower material needs and lower capital investments in manufacturing machinery (savings up to 40% are claimed to be possible);
- **high mechanical robustness**, allowing operation at very broad speed ranges, up to very high speeds;
- **compactness**, allowing highly dynamic applications, with low rotor inertia;
- **high reliability**, because the probability of faults between phases is low and because faults can hardly cause serious damage;
- **ease of repair**, because a concentrated stator winding can be easily accessed without interfering with others.

Besides the above advantages, the SRM has some shortcomings that discourage its use in many situations. The most apparent drawbacks are perhaps its torque pulsation, which can only be reduced with a more elaborate current control, and the necessity of position feedback for the motor to operate at all. These factors are currently preventing the SRM from being applied, for example, in mass-produced consumer goods, general-purpose drive systems or servodrives.

The SRM is finding application in fields where its inherent robustness and associated advantages can outbalance its deficiencies. Examples of such applications are conveyor systems ranging from 35 to 300 kW in the mining industry, as described in [28]. Elbuluk [24] and Radun [79, 81] have also reported the tendency of using SRMs in the aerospace industry, as "power-by-wire" actuators, in fuel pumps and as starter-generators. The ability of the SRM to operate at wide speed ranges can also be favourably exploited in high-speed direct-drive applications, enabling the elimination of gearboxes and the fabrication of more compact drives. This suits very well to applications such as medium-power pumps, fans, compressors, centrifuges and high-speed spindles. Battery-operated vehicles like fork lifts or small electric cars could also benefit from SR technology [46].

V_s	supply voltage	$[V_s] = V$
VSC	voltage-source converter	
VSI	voltage-source inverter	
W	energy	[W] = J
ZCS	zero-current switching	
ZVS	zero-voltage switching	
ZVS-CV	zero-voltage switching, clamped-voltage	
Z_r	characteristic impedance of a resonant circuit	$[Z_r] = \Omega$

P_L	losses in the resonant inductor	$[P_L]$ = W
PLR	parallel-loaded resonant	
PRACL	parallel resonant AC link	
PRDCL	parallel resonant DC link	
P_{sh}	losses in the upper switch	$[P_{sh}]$ = W
P_{sl}	losses in the lower switch	$[P_{sl}]$ = W
P_{SRM}	output power produced by SRM	$[P_{SRM}]$ = W
P_{sw}	switching losses	$[P_{sw}]$ = W
PT	punch-through	
P_{total}	total semiconductor losses	$[P_{total}]$ = W
PWM	pulse width modulation	
Q	quality factor	$[Q]$ = 1
r_s	internal stator radius	$[r_s]$ = m
R	resistance	[R] = Ω
$\boldsymbol{R}$	vector of phase winding resistances	$[\boldsymbol{R}]$ = Ω
R_θ	thermal resistance	$[R_\theta]$ = K/W
RMS	root mean square	
S	apparent power in general	$[S]$ = VA
S	switching device	
S_a	auxiliary switch	
S_c	clamp switch	
SCR	silicon controlled rectifier	
S_h	upper switch in an asymmetric bridge	
S_l	lower switch in an asymmetric bridge	
S_m	main output switch	
SOA	safe operating area	
S_s	shorting switch	
S_T	total apparent power rating	$[S_T]$ = VA
SLR	series-loaded resonant	
SR	switched reluctance	

i_{sh}	current through the upper switch	$[i_{sh}]$ = A
i_{sl}	current through the lower switch	$[i_{sl}]$ = A
I	current in general	[I] = A
I_c	clamp circuit turn-off current level	$[I_c]$ = A
I_{co}	initial clamp current	$[I_{co}]$ = A
I_d	current through the smoothing inductance	$[I_d]$ = A
IGBT	insulated gate bipolar transistor	
IM	induction machine	
I/O	input/output	
I_o	initial current for the boost period	$[I_o]$ = A
I_o	RMS output current	$[I_o]$ = A
I_T	trip current level	$[I_T]$ = A
j	adimensional counter	$[j]$ = 1
J_L	load moment of inertia	$[J_L]$ = kg·m^2
J_{SRM}	rotor moment of inertia of a SRM	$[J_{SRM}]$ = kg·m^2
k	adimensional multiplying factor, adimensional counter	$[k]$ = 1
k_0	adimensional coefficient of IGBT turn-on loss approximating function	$[k_0]$ = 1
k_1	temperature coefficient of IGBT turn-on loss approximating function	$[k_1]$ = 1/°C
k_b	boost factor	$[k_b]$ = 1
k_c	clamp factor	$[k_c]$ = 1
k_h	hardness factor	$[k_h]$ = 1
k_r	relief factor	$[k_r]$ = 1
L	inductance	$[L]$ = H
L	length	$[L]$ = m
L_c	C-dump chopper inductance	$[L_c]$ = H
L_d	smoothing inductance	$[L_d]$ = H
L_m	motor phase winding inductance	$[L_m]$ = H

A_{rms}	RMS surface current density	$[A_{rms}] = A/m^2$
AC	alternating current	
ACRDCL	actively clamped resonant DC link	
AQRDCL	auxiliary quasi-resonant DC link	
ARCP	auxiliary resonant commutated pole	
b_0	adimensional coefficient of IGBT on-state voltage drop approximating function	$[b_0] = 1$
b_1	temperature coefficient of IGBT on-state voltage drop approximating function	$[b_1] = 1/°C$
B	viscous friction coefficient	$[B] = Nms$
B_g	peak air gap magnetic flux density	$[B_g] = T$
B_g^{IM}	peak air gap magnetic flux density of an induction machine	$[B_g^{IM}] = T$
B_g^{SRM}	peak air gap magnetic flux density of a switched reluctance machine	$[B_g^{SRM}] = T$
BJT	bipolar junction transistor	
B_{sat}	magnetic flux density at saturation	$[B_{sat}] = T$
c	voltage coefficient of diode forward voltage drop approximating function	$[c] = V/A$
C	capacitance	$[C] = F$
CFM	converter-fed machine	
C_c	clamp capacitance	$[C_c] = F$
C_d	voltage divider capacitance	$[C_d] = F$
C_r	resonant capacitance	$[C_r] = F$
CRPWM	current-regulated pulse width modulation	
CSC	current-source converter	
d	exponent of diode forward voltage drop approximating function	$[d] = 1$
D_c	clamp diode	
D_i	mean diameter at the air gap	
D_h	upper diode in an asymmetric bridge	

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