Investigation of a drive system: soft-switching converter and switched reluctance motor

vorgelegt von
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ABSTRACT

The use of soft-switching converters in association with switched reluctance motors (SRM) potentially allows the fabrication of motor drives with increased power density and with better efficiency than other types of drive system. In applications where compact and lightweight drives are required, this kind of system can favourably compete with other drive types. Additionally, the SRM can be operated with high reliability at very high speeds in harsh environments, making it a good choice for specific applications such as fuel pumping in air-planes and several different uses in the mining industry. In this work, the feasi-bility of soft-switched reluctance drives is investigated and suitable soft-switching converter topologies for use in SRM drive systems are evaluated. A comparison between an actively-clamped resonant DC link SRM converter and a conventional hard-switched SRM converter is presented, and the potential size reduction due to the use of soft-switching is then estimated, as well as its overall losses, for a medium-power SR drive system.

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LIST OF SYMBOLS AND ABBREVIATIONS

δ	conduction angle	$[\delta] = °$
ΔV	voltage difference	$[\Delta V] = V$
ε	energy conversion ratio of a SRM	$[\varepsilon] = 1$
η	efficiency	$[\eta] = 1$
μ_o	permeability of air	$\mu_o = 4\pi 10^{-7}$ H/m
θ	rotor position	$[\theta] = °$
θ_d	dwell angle	$[\theta_d] = °$
θ_e	extinction angle	$[\theta_e] = °$
θ_k	k^{th} position data point	$[\theta_k] = °$
θ_{k-1}	$(k-1)^{th}$ position data point	$[\theta_{k-1}] = °$
θ_o	rotor position at the start of overlap	$[\theta_o] = °$
θ_{off}	turn-off angle	$[\theta_{off}] = °$
θ_{on}	turn-on angle	$[\theta_{on}] = °$
ω	angular speed	$[\omega] = 1/s$
ω_r	natural angular frequency of resonant circuit	$[\omega_r] = 1/s$
ξ	dummy integration variable	
ψ	flux linkage in general	$[\psi] = Wb$
$\boldsymbol{\psi}$	vector of phase flux linkages	$[\boldsymbol{\psi}] = Wb$
$\psi_{j,k}$	flux linkage for the j^{th} current data point and the k^{th} position data point	$[\psi_{j,k}] = Wb$
$\psi_{j-1,k}$	flux linkage for the $(j-1)^{th}$ current data point and the k^{th} position data point	$[\psi_{j-1,k}] = Wb$
ψ_k	flux linkage of phase *k*	$[\psi_k] = Wb$
ψ_{max}	peak flux linkage	$[\psi_{max}] = Wb$
a	cross-section radius of a toroid	$[a] = m$
a_0	coefficient of IGBT on-state voltage drop approximating function	$[a_0] = V/A$
a_1	temperature coefficient of IGBT on-state voltage drop approximating function	$[a_1] = V/A°C$

D_l	lower diode in an asymmetric bridge	
D_s	shunt diode	
DC	direct current	
DSP	digital signal processor	
EMC	electromagnetic compatibility	
EMI	electromagnetic interference	
E_{off}	IGBT turn-off energy loss	$[E_{off}]$ = J
E_{on}	IGBT turn-on energy loss	$[E_{on}]$ = J
ESL	equivalent series inductance	[ESL] = H
ESR	equivalent series resistance	[ESR] = Ω
f_r	natural frequency of resonant circuit	$[f_r]$ = Hz
f_s	sampling frequency	$[f_s]$ = Hz
$\overline{f}_{sw}$	mean switching frequency	$[\overline{f}_{sw}]$ = Hz
FET	field-effect transistor	
g	mean radius of a toroid	$[g]$ = m
GTO	gate turn-off thyristor	
h_0	coefficient of IGBT turn-on loss approximating function	$[h_0]$ = J/A
h_1	temperature coefficient of IGBT turn-on loss approximating function	$[h_1]$ = J/A°C
i	instantaneous current	$[i]$ = A
$\boldsymbol{i}$	vector of phase currents	$[\boldsymbol{i}]$ = A
i_{dh}	current through the upper diode	$[i_{dh}]$ = A
i_{dl}	current through the lower diode	$[i_{dl}]$ = A
i_j	j^{th} current data point	$[i_j]$ = A
i_{j-1}	$(j-1)^{th}$ current data point	$[i_{j-1}]$ = A
i_{Lr}	current through the resonant inductor	$[i_{Lr}]$ = A
i_m	motor current	$[i_m]$ = A
i_{max}	peak phase current	$[i_{max}]$ = A
i_o	output current	$[i_o]$ = A

L_r	resonant inductance	$[L_r]$ = H
LSB	least significant bits	
L_{stk}	stack length	$[L_{stk}]$ = m
m	number of phases	[m] = 1
m_0	coefficient of IGBT turn-off loss approximating function	$[m_0]$ = J/A
m_1	temperature coefficient of IGBT turn-off loss approximating function	$[m_1]$ = J/A°C
MCS	motion control systems	
MCT	MOS controlled thyristor	
MIPS	million instructions per second	
MLC	multi layer ceramic	
MOS	metall oxide - semiconductor	
MOSFET	MOS field-effect transistor	
n	n-type doped semiconductor	
n_0	adimensional coefficient of IGBT turn-off loss approximating function	$[n_0]$ = 1
n_1	temperature coefficient of IGBT turn-off loss approximating function	$[n_1]$ = 1/°C
n_L	number of lower switches	$[n_L]$ = 1
n_s	rated rotor speed	$[n_s]$ = 1
n_U	number of upper switches	$[n_U]$ = 1
N	number of turns	[N] = 1
N_p	number of turns per pole	$[N_p]$ = 1
NPT	non punch-through	
N_r	number of rotor poles	$[N_r]$ = 1
p	p-type doped semiconductor	
P	power in general	$[P]$ = W
P_{dh}	losses in the upper diode	$[P_{dh}]$ = W
P_{dl}	losses in the lower diode	$[P_{dl}]$ = W
PI	proportional + integral	

SRACL	series resonant AC link	
SRDCL	series resonant DC link	
SRM	switched reluctance motor	
t	time	$[t]$ = s
T	temperature	$[T]$ = °C
T	torque	$[T]$ = Nm
T_{boost}	duration of the boost period	$[T_{boost}]$ = s
T_{clamp}	duration of the clamp period	$[T_{clamp}]$ = s
T_e	electromagnetic torque	$[T_e]$ = Nm
T_f	current fall time at turn-off	$[T_f]$ = s
T_{fall}	duration of the falling resonant transition	$[T_{fall}]$ = s
T_L	load torque	$[T_L]$ = Nm
T_{peak}	peak torque	$[T_{peak}]$ = Nm
T_{rise}	duration of the rising resonant transition	$[T_{rise}]$ = s
v	instantaneous voltage	$[v]$ = V
$\boldsymbol{v}$	vector of phase voltages	$[\boldsymbol{v}]$ = V
v_{Cc}	voltage accross the clamp capacitor	$[v_{Cc}]$ = V
v_{CE}	IGBT on-state voltage drop	$[v_{CE}]$ = V
v_{Cr}	voltage accross the resonant capacitor	$[v_{Cr}]$ = V
v_f	diode forward voltage drop	$[v_f]$ = V
V	voltage in general	[V] = V
V_0	voltage coefficient of IGBT on-state voltage drop approximating function	$[V_0]$ = V
V_1	temperature coefficient of IGBT on-state voltage drop approximating function	$[V_1]$ = V/°C
V_{BR}	breakdown voltage	$[V_{BR}]$ = V
V_F	coefficient of diode forward voltage drop approximating function	$[V_F]$ = V
V_i	mean input voltage	$[V_i]$ = V
V_o	mean output voltage	$[V_o]$ = V

1 Introduction

In many motion control applications, it is desirable to attain a high power density. In other words, excessive weight and volume are mostly unwanted characteristics in a motion control system (MCS). Other important properties of a MCS are high efficiency, reliability and good electromagnetic compatibility (EMC) [104]. However, some of these requirements are frequently conflicting. Therefore, an improved EMC, for example, would demand the use of larger filter circuits, thus increasing the size and the cost of the drive system.

Among the many possible components of a MCS, some that contribute markedly to unwanted bulkiness are:

- the electric motor(s);
- the power electronic converter circuits;
- the cooling devices.

Lipo [55] has shown that electric motors of higher power density can be constructed "based on the principle of using a switching power converter to deliver currents of optimum waveform to match that of the emf of energy conversion within the machine". He points out the switched reluctance motor (SRM) as the precursor of this family of machines, which he termed "converter-fed machines" (CFM). As the first successful SR drive system was announced [47], it caused great enthusiasm among researchers in the field of electrical drives. That was the first successful attempt of a strictly converter-fed machine featuring highly non-sinusoidal air gap flux at saturation levels, with power densities comparable to that of induction machines. Furthermore, its very simple mechanical construction, with concentrated stator windings and without any windings or magnets in the rotor, seemed to offer many benefits [60]:

- **higher efficiency**, due to lower rotor losses (this allows increasing the power density even further);

In low to medium-power ranges, further power-density enhancement of motion control systems could be achieved if the motor and the power electronic converter could be mechanically integrated into a single unit. This appears to be a natural tendency, as converter technology continuously improves [104]. However, this requires a drastic size reduction of the power electronic circuitry. To increase the power density of a converter, it is necessary to reduce its losses and raise its switching frequency. At higher switching frequencies, the size of electromagnetic energy storage components like filter inductors and DC link capacitors can be significantly reduced. Lowering the converter's overall losses can also make it possible to reduce its size by using smaller cooling devices. However, in order to raise the switching frequency, it is also necessary to have lower *switching* losses in the power semiconductor switches. Theoretically, reduction of semiconductor losses can be achieved by designing new and improved power semiconductor devices that exhibit lower on-state voltage drop and inherently lower switching losses. Nevertheless, reduction of switching losses of existing switches can be achieved through soft-switching [21]. The principle of soft-switching consists on making that, at each power semiconductor switch:

- the voltage falls to zero before the current begins to rise at turn-on (as is done in zero-voltage switching (ZVS) circuits), or
- the current falls to zero before the voltage begins to rise at turn-off (as is done in zero-current switching (ZCS) circuits).

This can be accomplished by adding small undamped LC networks at strategic places in the converter circuit and gating the power semiconductor switches on and off at the right opportunities.

In contrast to soft-switched converters, other power electronic converters can be classified as hard-switched. Fig. 1.1 shows typical switching loci of both converter types on the $V \times I$ plane. In hard-switched converters, high switching losses occur when the converter drives an inductive load. Due to diode reverse recovery, the current rises very fast at turn-on and overshoots the load current by a considerable amount. As the voltage across the switch takes some time to

that are best matched by SR machines. The combination of soft-switched converters and switched reluctance machines can thus result in a drive system that is best suited for these kind of application, and the perception of this fact has given the motivation for this work.

1.1 Objectives and overview of this work

This work has the main purpose of evaluating the potential for the development of high power density electric motor drives consisting of switched reluctance machines and soft-switched converters. As intermediary objectives, the following topics can be pointed out:

- analysis of known soft-switching converter topologies and assessment of their suitability for application in SR drive systems;
- development of a simulation model for soft-switched SR drives and design of a soft-switched SR drive with help from simulations, using a freely available simulation program;
- construction of a prototype soft-switched SR drive, based on the preceding design, implemented with a minimum of control hardware using a DSP controller and control software, including phase commutation, speed and current control, supervisory and protective functions;
- experimental validation of the developed simulation model, comparing simulation results with experimental measurements;
- theoretical calculation of potential size reduction of an SR converter, due to the power loss reduction associated to the use of soft switching, taking into consideration the technological characteristics of the components.

In chapter 2, the SRM design and operation aspects which are relevant for the development of a drive system with the above properties are summarized, and guidelines for the design of the power electronic controller are presented.

In chapter 3, a comparative study of soft-switching converter topologies is presented and appropriate topologies for use with SRMs are pointed out.

2 Switched Reluctance Drives

The SRM operation is based on the principle of the minimum reluctance, which is a corollary of the physical law of minimum energy, i.e., a movable mechanical system subject to a magnetic field tends to find a position where the energy stored in the magnetic field is a minimum. At this position, the reluctance of the magnetic circuit is also a minimum, and the inductance seen by the exciting electrical circuit is a maximum. The operating principle of the switched reluctance machine is well-known and since last century many people have attempted to construct motors based on this principle [60]. However, it was not until 1980 [47] that the first successful high-performance SRM drive system was announced. This drive system used a power electronic converter to commutate the phase currents according to the rotor position. This allowed for the full utilization of the motor's torque producing capability. As a result, it was claimed that the SRM could compete with the squirrel cage induction motor and even supersede it in most applications, due to the high attainable torque and power per volume. Numerical data on this subject are given at the end of the following section.

2.1 Design Characteristics of the SRM

The mechanical construction of the SRM is very uncomplicated. Both the stator and the rotor are laminated and have an even number of salient poles. Fig. 2.1 shows the cross section of a three-phase SRM, with six stator poles and four rotor poles (also called 6/4 SRM). The motor which has been used in the experimental part of this work has this configuration. Details of its design can be taken from Appendix I. A concentrated winding is mounted around each stator pole and the rotor carries neither windings nor magnets. Windings of opposite poles are connected together to form a phase, in such a way that their fluxes are additive, as indicated by the dots and crosses in Fig. 2.1. The rotor position displayed in Fig. 2.1 is defined as the aligned position with respect to

Unlike other kinds of electric machine, the switched reluctance machine is normally designed to operate close to saturation [60, 80]. In fact, a well-designed SRM will exhibit local saturation at the overlapping pole-corners, which typically occurs at peak air gap flux density magnitudes of 1.2 – 1.7 T. This is a desirable feature, because it maintains a nearly fixed flux density at the overlapping pole-corners and this has a positive effect upon the torque production. In this case, saturation will have the beneficial side effect of reducing the required iron volume for a given torque and reducing the motor VA requirements for a given output power, as will be discussed further below. However, saturation of the back iron is undesirable, because it will only increase the magnetizing current, without contributing to an enhancement of the torque production. For conventional soft magnetic material used for motor laminations, the magnetic flux density at onset of saturation is, nearly, B_{sat} = 1.7 T. With this value of flux density, the peak torque produced by a SRM is approximately given by [60]:

$$T_{peak} = B_{sat} r_s L_{stk} \cdot 2N_p i, \tag{2.1}$$

where N_p is the number of turns per pole, r_s is the internal stator radius and L_{stk} is the stack length of the laminations, both in meters.

In [55], the following sizing equation for a SRM without any special cooling (naturally air-cooled) is proposed, for the purpose of comparing the maximum power density theoretically obtainable from a SRM and from an induction machine:

$$P_{SRM} = \frac{7\sqrt{3}\,\pi^2}{2160}\,\eta\, B_g\, A_{rms}\, n_s\, (D_i^2 L), \tag{2.2}$$

where $D_i^2 L$ is the volume of the machine at the air gap (m^3), A_{rms} is the RMS surface current density (A/m^2), B_g is the peak air gap flux density (T), n_s is the rated speed (min^{-1}), and η is the total machine efficiency. Many considerations about the machine geometry, like pole arcs and winding geometry are implicit

tions and the audible noise caused by its doubly-salient mechanical structure. Reduction of the torque pulsations through active phase current waveform shaping reduces also the efficiency of the SRM. Audible noise is more difficult to be reduced by phase current control. Audible noise in SRMs is mainly provoked by radial deflection of the stator, due to the high radial component of the attracting forces between the rotor and stator poles. The most effective way of reducing this kind of noise is designing SRMs with stiffer structure. Other sources of audible noise are vibration of the phase windings and magnetostriction. Winding vibration can be reduced by a more stable mechanical assembly. Magnetostriction noise depends on the silicon content of the laminations and is approximately zero for a percentage of about 7% of silicon in the steel [32]. In any case, if the phase currents are regulated with a small current ripple, the audible noise is also reduced. Guidelines for the reduction of audible noise of SRMs can be found in [106].

Due to the highly non-linear characteristics of the SRM, it is difficult to predict its dynamic behaviour with simple analytic calculations. In any case, one has to know its non-linear magnetization characteristics in order to calculate its generated torque and counter-emf [94]. One method of obtaining the magnetization characteristics of a SRM is through computer-aided finite-element field calculation. Fig. 2.2 shows typical magnetization curves for one phase of a switched reluctance machine, obtained from two-dimensional finite-element field calculation (which is sufficient in most cases). These calculations have been done with the program 3DFE, which has been developed by Jänicke [37] as his Ph.D. work at the Institute of Electrical Machines, at the University of Technology Berlin. The uppermost curve in Fig. 2.2 (a) corresponds to the situation where the rotor poles are aligned with the stator poles of that phase (aligned position) and this is defined as position zero in Fig. 2.2 (b). The lowest curve in Fig. 2.2 (a) refers to the unaligned position, defined as position -45° in Fig. 2.2 (b). The negative angle values refer to rotor positions *before* the aligned position, for a given sense of rotation. The position definitions are based on a rotor coordinate system, hence the angle units are mechanical degrees. This coordinate system is used throughout this work for all angle values.

The torque produced by each phase can be calculated from the magnetization data by the partial derivative of the magnetic co-energy with respect to the mechanical angular displacement of the rotor. Alternatively, the torque can be obtained from the expression of the Maxwell tensor $\vec{T}$ ([T] = [N/m^2]):

$$\vec{T} = \left(\vec{n} \cdot \vec{H}\right)\vec{B} - \vec{n}\frac{1}{2}\left(\vec{B} \cdot \vec{H}\right), \tag{2.3}$$

as is the case in the program 3DFE. At a first approximation, based on the two-dimensional field model, the torque can be calculated by simply multiplying the tangential component of $\vec{T}$ by the stack length. Typical SRM torque characteristics, calculated from the Maxwell tensors obtained with the program 3DFE, are shown in Fig. 2.3.

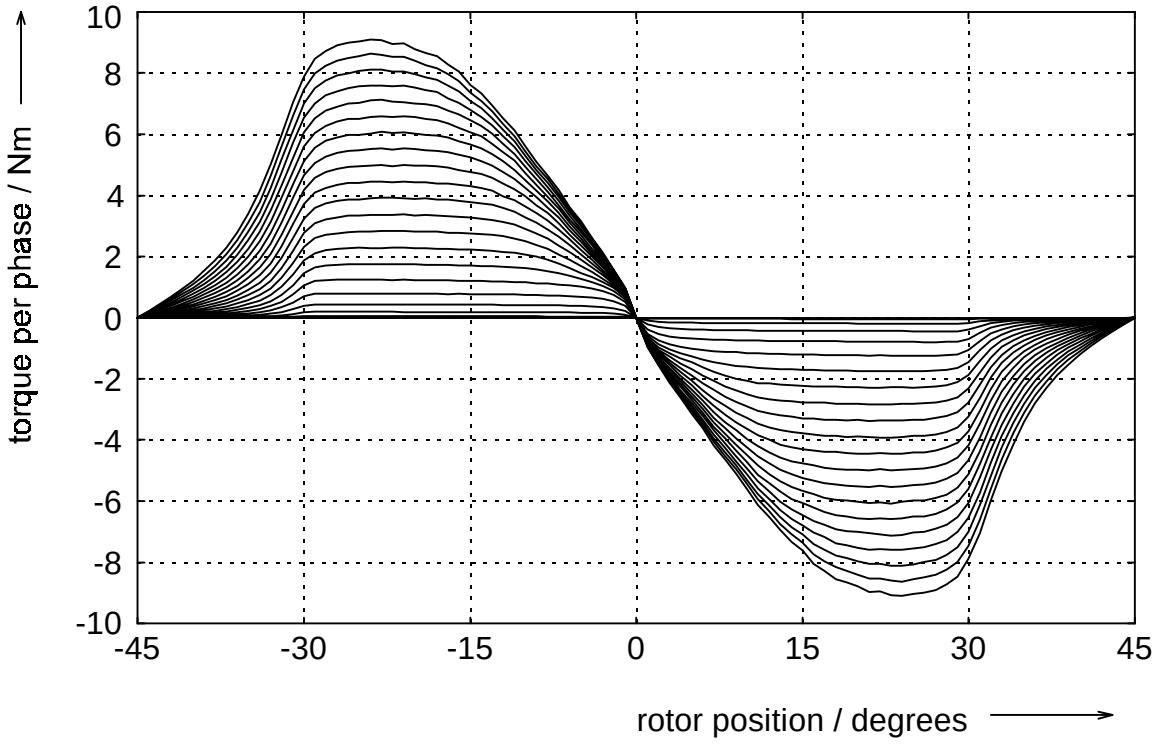


Fig. 2.3: Typical torque vs. rotor position for a SRM at different current magnitudes between 0A (lower trace) and 20A (upper trace), at 1A intervals.

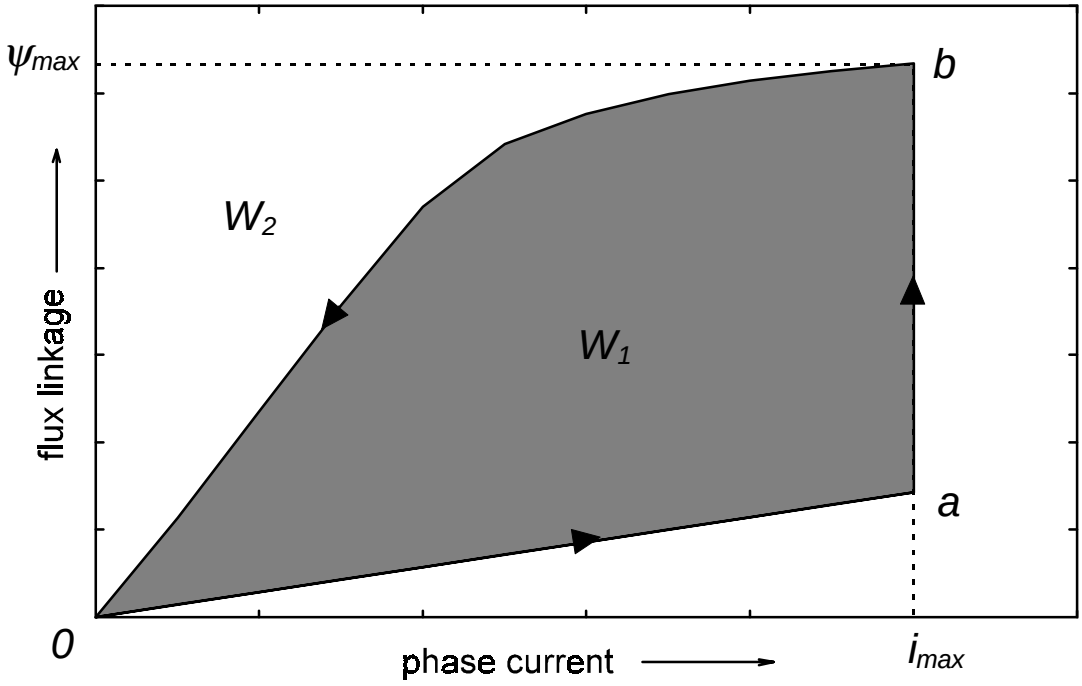


Fig. 2.4: Ideal energy-conversion loop
W_1: converted energy;
W_2: recovered energy.

In a real SR drive, the energy-conversion loop will change according to the rotor speed and to the mode the driving circuit is operated. However, it will always enclose a smaller area than the ideal energy-conversion loop, as described in [60]. This happens because the rotor moves by a considerable amount during the times needed to turn the phase current on and off, especially at higher speeds. It has been shown in [60] that the peak value of flux-linkage ψ_{max} reached during one phase stroke, assuming a nearly linear increase of the flux-linkage during the magnetization period, is approximately given by:

$$\psi_{max} = \frac{V_s \delta}{\omega}, \tag{2.4}$$

where V_s is the supply voltage, δ is the conduction angle of the phase until it is turned off and ω is the angular speed of the machine.

$$S = V_s\, i_{max} = \frac{\omega\, W_1}{k\, \varepsilon\, \delta} \quad . \tag{2.8}$$

This relation can be directly used to determine the total VA rating of converters for SRMs, as discussed in Section 2.3.

2.2 Mathematical Description of the SRM

To derive a mathematical model for the SRM, the following simplifying assumptions are made:

- mutual coupling between phases is negligible;
- hysteresis and eddy current losses in the magnetic circuit are neglected;
- the winding resistance is assumed to be constant and independent of the current waveform or frequency.

Under the above assumptions, the dynamical behaviour of the SRM can be described by the following set of equations:

$$T_e(\theta, i) = \sum_{k=1}^{m} \left(\frac{\partial}{\partial \theta} \int_0^{i_k} \psi_k(\theta, \xi)\, d\xi \right); \tag{2.9}$$

$$\boldsymbol{v} = \boldsymbol{R}^{T} \cdot \boldsymbol{i} + \frac{d\boldsymbol{\psi}}{dt}; \tag{2.10}$$

where m is the number of phases; $\boldsymbol{v}$, $\boldsymbol{R}$, $\boldsymbol{i}$ and $\boldsymbol{\psi}$ are $[m \times 1]$ vectors of voltage, resistance, current and flux linkage for all phases; θ is the rotor position; T_e is the total electromagnetic torque and $\psi_k = \psi_k(\theta, i)$ is the flux linkage of each phase.

The mathematical model is completed by a differential equation describing the movement of the shaft with an attached mechanical load. For example, if the

- it should allow an overlap of the phase currents, i.e. more than one phase can conduct current at a time. It is usually desired when the machine is operated at high speeds, because the time available for the phase currents to fall to zero after commutation is too short. In this case, phase current overlap permits smoother operation;
- it should be capable of applying pulses of reverse voltage on a phase when it is turned off or commutated to the next phase, in order to make the current to fall quickly to zero. This provides a fast demagnetization of the offgoing phase, minimizing the negative torque production which occurs if current flows after the rotor has passed the aligned position for that phase.

Fig. 2.5 shows one phase of the "asymmetric bridge" converter topology, which is also termed "classic" converter configuration by some authors [102]. It can be used with machines of any phase number, simply by connecting as many independent sections (Fig. 2.5) as needed in parallel with the DC supply. This converter provides a high degree of control flexibility, because the current control can be totally independent for each phase, allowing operation with any desired phase overlapping. It also provides extra reliability to the SR drive system, in addition to the inherent higher reliability already provided by the SR machine, because it does not permit a short-circuit of the DC bus through the main switches (shoot-through), since the phase winding is series-connected between the main switches. However, this configuration is not the most economical one, because it requires two power switches for each phase. There are other topologies which use less than two switches per phase, but they generally exhibit some limitations in comparison to the "classic" topology, as discussed further below.

active. This provides a free-wheeling path for the phase current, allowing operation with lower current ripple or lower switching frequency.

Unfortunately, the above terminology can be easily confused with the expressions "hard switching" and "soft switching". However, as both terminologies are already well established, it has not been attempted to create a new one, and the reader should therefore be attentive to the right meaning when they appear.

A comparison between the DC link current of a converter in the two operating modes described above is shown in Fig. 2.6. In both cases, the operating conditions are identical: the load torque, the speed the supply voltage and the commutation angles are the same, and the phase currents at the converter output are regulated to the same value (5A), with the same ripple. These results were obtained from simulations, which are more thoroughly discussed in section 5.1. It should be noted that the lower DC link current in the soft chopping mode allows the use of a smaller filter capacitance in the DC link, thus enabling some size reduction of the circuit.

The total VA rating of the "classic" converter is roughly given by $S_T = 2\ m\ S$, where S is the per-phase VA requirement of the SRM, given by equation (2.8). As an attempt to reduce the total required VA ratings of SRM converters, many authors have suggested innovative topologies as alternatives to the asymmetric-bridge configuration. The main idea of all these developments has been to reduce the number of controllable power semiconductor switches per phase, thus reducing the total converter VA ratings, with the consequent cost reduction. In some of these developments, however, inherent advantages of SRMs have been sometimes neutralized, or some insufficiencies have been worsened. This is the case, for instance, with the converter described in [42], in which the inherent impossibility of occurrence of shoot-through faults has been eliminated.

A converter which uses less than two switches per phase will not necessarily exhibit a total VA rating lower than the classic asymmetric bridge converter, as can be seen from the example of the converter for bifilar SRMs, shown in Fig. 2.7. In this topology, only one controllable switch per phase is used, but the voltage rating of the power semiconductors must be at least twice the supply voltage, because of the magnetic coupling between the windings. For the same current rating, the total converter VA rating will be roughly the same as that of the classic converter.

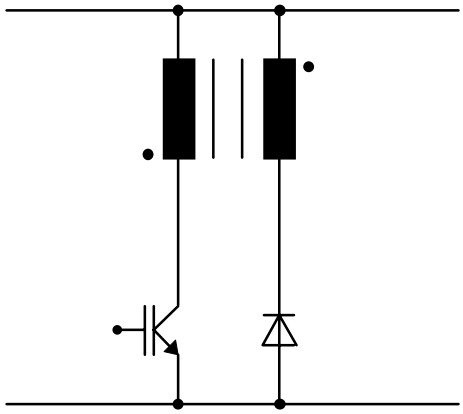


Fig. 2.7: One phase of a bifilar-winding SRM converter.

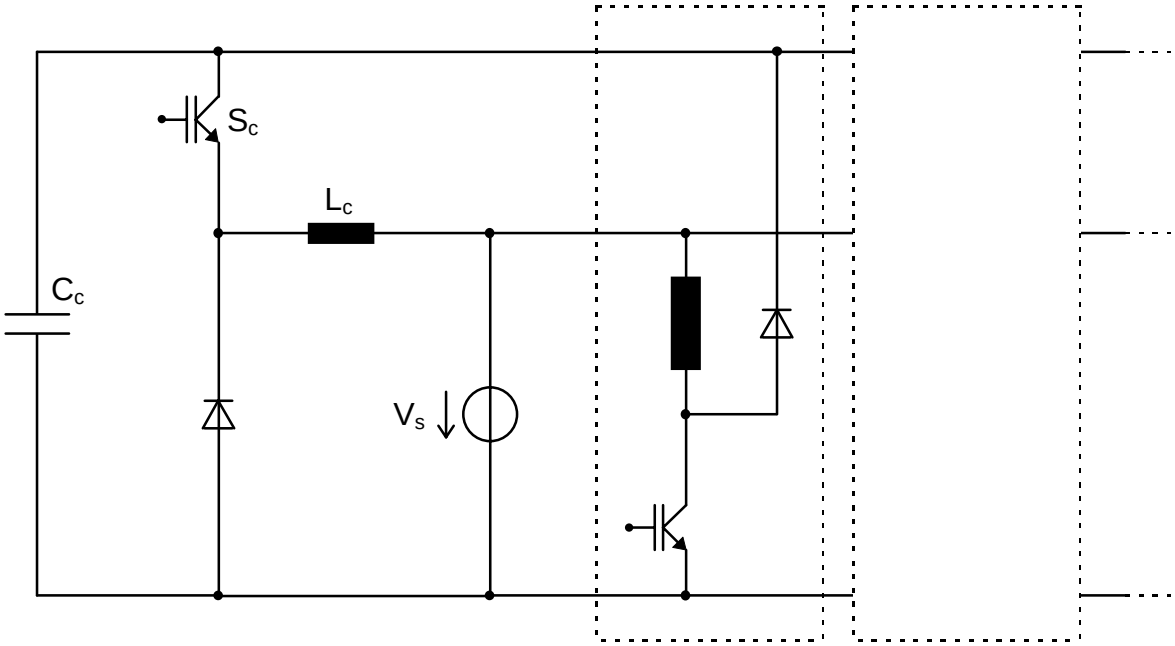


Fig. 2.8: C-dump converter.

Fig. 2.9 shows the schematic diagram of a split-supply converter, also known as "Oulton" converter. This converter has been developed for the first commercially available general-purpose SR drive system, the Oulton™ drive. The total component VA rating of the Oulton converter is also approximately the same as that of the asymmetric bridge converter, because the supply voltage must be rated at twice the rated motor voltage. Furthermore, this converter exhibits following disadvantages:

- an unbalance of the phase currents will lead to an unequal distribution of the supply voltage between the splitting capacitors;
- the circuit is only suitable for machines with an even number of phases;
- the source voltage is not fully utilized;
- only hard-chopped operation is possible.

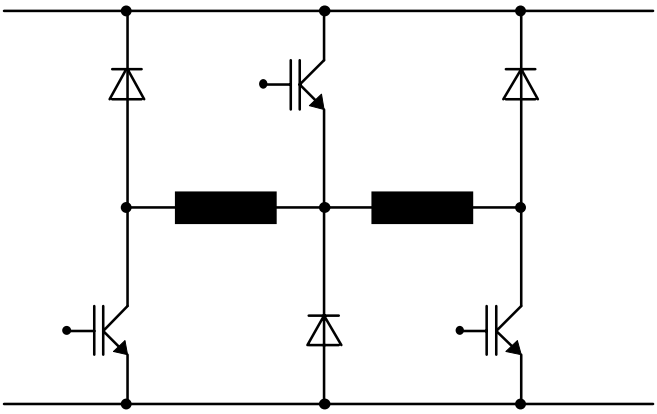


Fig. 2.10: Section of the "Pollock" converter.

The Pollock converter can be best used with four-phase SRMs, because in this case two structures like that of Fig. 2.10 can be used in an interleaved manner, with two non-adjacent phase windings in each section. If the phase current overlap is low, so that at most two adjacent phases conduct current at a time, thus the controllability will be as good as that of the "classic" converter. Additionally the voltage rating of the power semiconductor switches is the same for both topologies. As a result, the total VA rating of the Pollock converter will be only 3/4 of the VA rating of the "classic" converter for four-phase SRMs.

Another shared-switch topology known as "Miller" converter is shown in Fig. 2.11. In this circuit, only one power switch is shared and it undertakes the task of controlling the current of all phases. It is capable of operating in soft-chopping mode, but the phase currents cannot be controlled if some other phase is being demagnetized. The main advantage of this circuit is the lower VA rating compared to the "classic" topology, by a factor $(m+1)/2m$.

2.4 System Operation

2.4.1 Phase Current Commutation

For one phase winding of a SRM to produce motoring torque, current must flow in the winding while its inductance is increasing with the change in the rotor position. This is the region between the positions $-\frac{\pi}{N_r}$ and *0* in Fig. 2.12, which shows typical waveforms for single-pulse operation. At $\theta = \theta_o$, the rotor and stator poles start to overlap, and the inductance begins to increase very rapidly. The phase current should be at best turned on before θ_o (at $\theta = \theta_{on}$), in order to allow a faster current rise. The current rises faster for $\theta < \theta_o$ because of the lower counter-emf in this region, associated to the small variation of the flux-linkage with both phase current and rotor position (cf. Fig. 2.2). The phase current should be turned off before the rotor reaches the aligned position ($\theta = 0$), in order to leave some time for the current to reduce to zero before the rotor enters the region of decreasing inductance, where braking torque is produced.

The current waveform shown in Fig. 2.12 is produced by a constant voltage applied to the phase winding, without current control. The interval between θ_{on} and θ_{off} , during which the phase winding is connected to the source through the main phase switch(es), is called "dwell" period. After commutation at $\theta = \theta_{off}$, the phase current falls, under the influence of a reverse phase voltage, until it becomes zero at the extinction angle $\theta = \theta_e$. The interval between θ_{off} and θ_e , during which the phase current returns to the source through the fly-back diode(s), is called "tail" period.

rent. However, the polarity of the counter-emf reverses at the aligned position, reducing the voltage difference available for demagnetization. This causes an inflection of the tail current waveform at $\theta = 0$, as shown in Fig. 2.12.

The magnitude of the counter-emf is a function of the instantaneous phase current, of rotor position and speed. At high speeds, the counter-emf can become higher than the applied reverse voltage past the aligned position, causing the tail current to start to increase again after commutation and degrading severely the motor performance. Hence, for optimum SRM operation, the commutation angles must be advanced as the speed increases. The determination of the optimum commutation instants is a cumbersome procedure and many (analytical and experimental) methods have been reported [1, 57, 100, 95]. Alternatively, the optimum commutation angles can be searched on-line, with an optimizing algorithm based on minimization of the DC link current [38]. One advantage of this method is that it does not requires a priori knowledge of motor flux-linkage and torque versus angle characteristics and avoids time-consuming off-line optimization calculations.

Depending on the motor geometry, optimum commutation will probably require some degree of overlap of the phase currents. However, distinction should be made between two types of overlap. In "tail overlap", it is the tail period of the preceding current pulse that overlaps into the dwell period of the following current pulse. In "dwell overlap", the superposition extends into the dwell period of both current pulses. Dwell overlap causes increased current stress on the DC link capacitor in comparison to tail overlap, as shown in Fig. 2.13 (b) and (e). Avoiding dwell overlap may allow the use of smaller DC link capacitors, because they do not need to be dimensioned to supply current for two phases simultaneously. But it can also aggravate the problem of torque dips at commutation and reduce the average output torque, as shown in Fig. 2.13 (c) and (f). An alternative commutation method consists on inserting a freewheeling period before the complete turn-off of a phase, beginning at the same time the following phase is turned on, as shown in Fig. 2.14. This method produces a less severe torque dip than the commutation without overlap (cf.

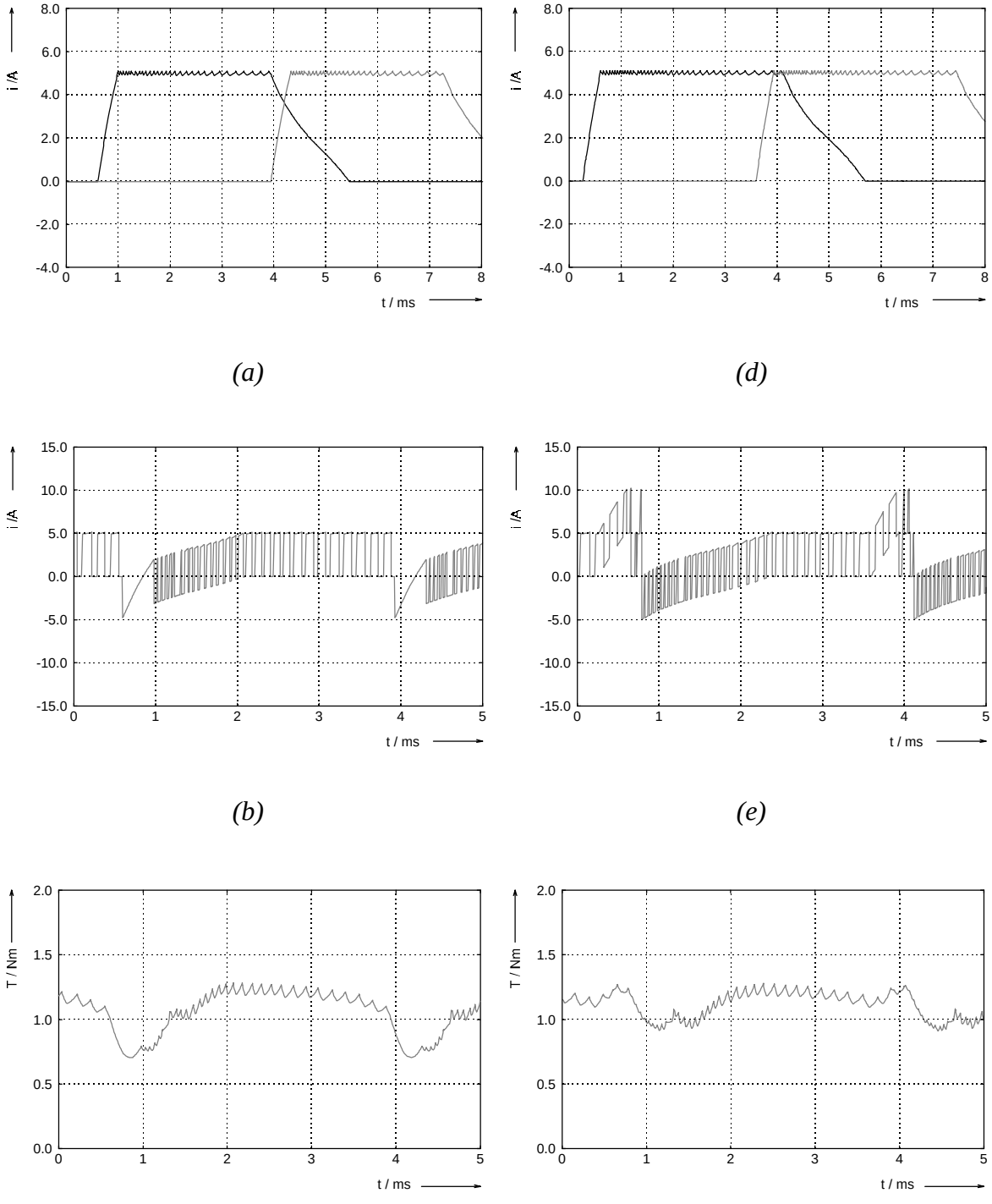


Fig. 2.13: Comparison between tail overlap (a,b,c) and dwell overlap (d,e,f) with current control in the dwell region (simulation results for 300V supply and 1500 rpm) (a),(d): phase currents; (b),(e): DC link current; (c),(f): output torque.

The achievement of high di/dt at the turn-off of a phase is also very important, in order to obtain a good performance from a SRM [53]. If the di/dt is too low, the phase current will extend further into the negative torque-producing region, reducing the total average torque produced by the machine. Moreover, if the phase current is turned off too early, in order to avoid a negative torque production, the contribution of each phase to the total torque can also be reduced, thus lowering the total average torque as well. Since the main phase inductance is high near the aligned position, the turn-off di/dt can be increased by means of applying a higher turn-off voltage. Fig. 2.15 shows the turn-on and turn-off paths of the phase current separately. In the classic converter topology, nodes *a* and *c* are connected together, as well as nodes *b* and *d*. As a result, the voltage at turn-off is the same as at turn-on in that configuration. The effect of different values of turn-off voltage on the phase current is shown in Fig. 2.16, for a turn-on voltage of 300V.

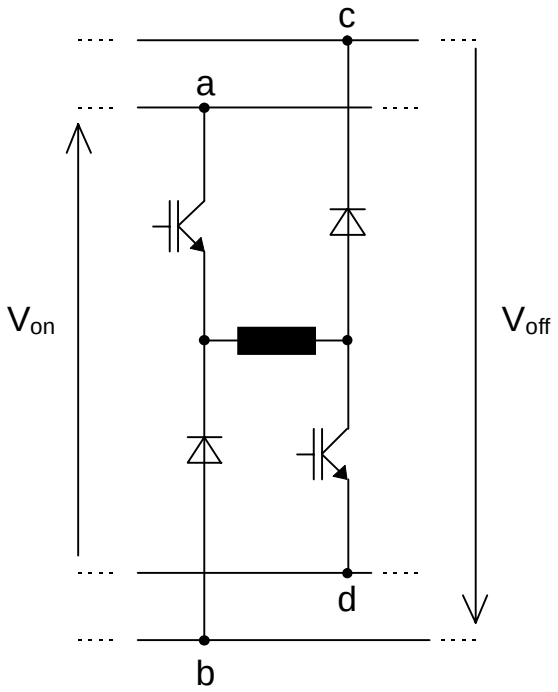


Fig. 2.15: Turn-on and turn-off (demagnetizing) voltage.

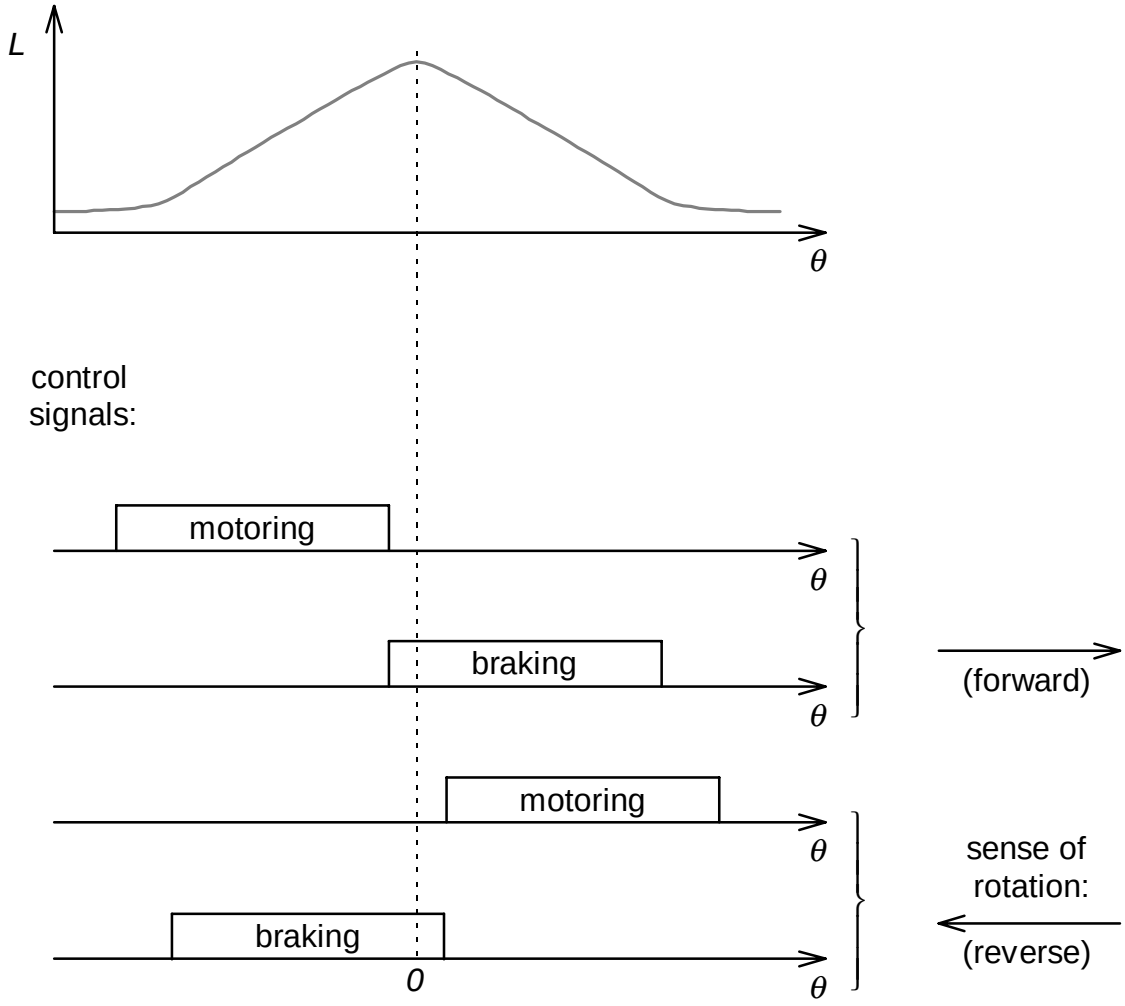


Fig. 2.17: Commutation signals for different operating modes.

If a controlled braking torque is required, the braking currents can be regulated by chopping the phase switches, as in motoring operation. However, current control can only be done by hard-chopping during braking operation. Furthermore, due to the increase of counter-emf with speed and current, there is an upper limit for the braking current which can be controlled. In other words, the maximum value of controllable braking current is a function of speed, but this relationship cannot be analytically determined. Although the polarity of the

3 Soft Switching Converters

In the early days of solid-state power electronics, thyristors were the only controllable power semiconductors available. Because they cannot be turned-off from the gate terminal, many ingenious auxiliary circuits have been developed, to allow thyristors to be used in power converters that could not be naturally commutated by the load or by the line voltage. Many circuits for thyristor forced commutation could be regarded as soft-switched, because they use controlled LC oscillations in order to reduce the current through the thyristor to zero before it can be turned off. The development of self-commutated power semiconductor switches with gate turn-off capability has led to the obsolescence of forced commutation, initiating the age of hard-switched converters. Further development of power semiconductor technology has allowed the fabrication of faster and more rugged power semiconductor switches, leading to an enhancement in switching frequency and power level of converters.

However, the higher power and switching speeds of the switches have caused an increase of switching stresses on the power semiconductor switches. The fast switching transitions at higher voltage and current levels excites the parasitic inductances and capacitances close to the converter switches, giving rise to excessive voltages, currents and power losses during the switching process. These switching stresses must be maintained under acceptable levels in order to keep the switching trajectory inside of the device's safe operating area (switching SOA) and therewith avoiding premature device failure. This can be accomplished by adding small inductances and capacitances to the circuit at the switch terminals, in order to slow down the rate of change of current and voltage on the switch, during the switching transitions. In this process, the small electromagnetic energy storage elements added to the circuit will trap some energy at each switching transition, and they must be reset at every cycle. The trapped switching energy can be dissipated in a resistor (as in a dissipative snubber circuit), recovered to the source (regenerative snubbing), or it can be returned to the main circuit, as is done in resonant converters. These three

  - Current-source parallel-resonant converters;
  - Class E and subclass E resonant converters.

- Resonant-Switch converters
  - Resonant-switch DC-DC converters:
    Zero-current-switching (ZCS) converters;
    Zero-voltage-switching (ZVS) converters.
  - Zero-voltage-switching, clamped-voltage (ZVS-CV) converters, which are also referred to as pseudo-resonant converters and resonant-transition converters.

- Resonant link converters
  - High-frequency-link integral-half-cycle converters (resonant AC link);
  - Resonant DC link converters.

The main characteristics of each of the above related soft-switching converter families is briefly described in the following sub-sections. A more detailed analysis of the most appropriate topologies for application in SR drive systems is then presented in section 3.2.

3.1.1 Load-resonant converters

For operation with load-resonant converters, an inductive load must be transformed in an LC resonant tank by adding capacitance and maybe also some additional inductance to the circuit. The resonant tank is excited by rectangular pulses of voltage, as in a series-resonant converter, or current, as in a parallel resonant converter. These pulses are supplied from a converter that is topologically identical to a hard-switching converter, in the sense that no additional LC elements are connected directly to the switches, as shown in Fig. 3.2. Soft-switching operation is achieved just by turning the switches on and off at the right instants. Taking the case of the series-resonant converter as an example

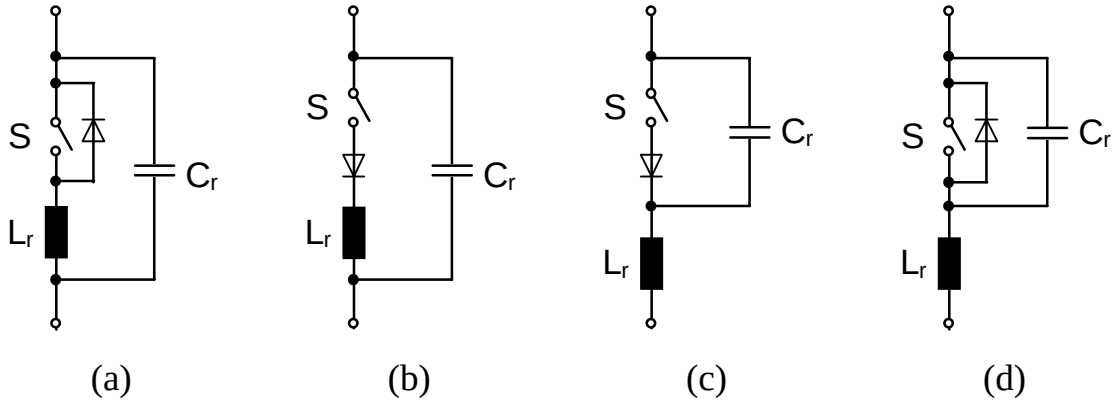
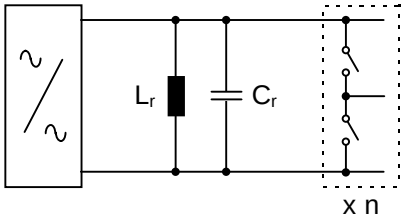
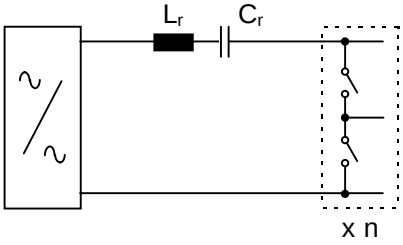
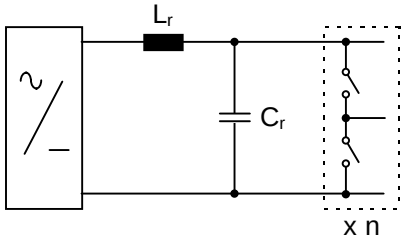
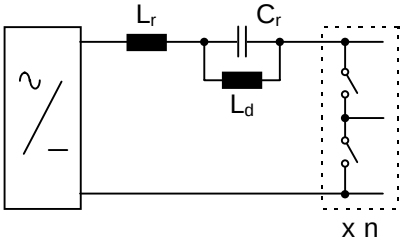
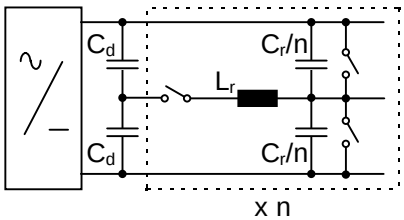


Fig. 3.3: Resonant-switch configurations:
(a) full-wave ZCS (zero-current switch);
(b) half-wave ZCS (zero-current switch);
(c) full-wave ZVS (zero-voltage switch);
(d) half-wave ZVS (zero-voltage switch).

For zero-current switching (ZCS) operation, the resonant inductor is directly connected in series with the semiconductor switch, as shown in Fig. 3.3 (a) and (b). The rate of rise of the current through the semiconductor switch is limited by the resonant inductor at turn-on. Additionally, the semiconductor switch can only be turned off when its current returns to zero, and this is provided by the free oscillation of the resonant tank. In the circuit of Fig. 3.3 (a), the current in the resonant inductor is allowed to flow in the reverse direction, yielding operation in the so-called full-wave mode. Conversely, the resonant inductor current is not allowed to reverse in the circuit of Fig. 3.3 (b), which operates in the half-wave mode. The ZVS resonant-switch configurations shown in Fig. 3.3 (c) and (d) are dual to the above described zero-current resonant switches. The presence of a resonant capacitor in parallel to the power semiconductor elements in these circuits obliges that they are turned on only when the voltage across the capacitor is zero. The full-wave ZVS switch shown in Fig. 3.3 (c) allows a negative excursion of the resonant capacitor voltage, but in the half-wave ZVS resonant-switch circuit of Fig. 3.3 (c), the capacitor voltage cannot undergo a negative oscillation. The control of the output power in resonant-switch converters is usually realized by use of frequency modulation. Some

tor VSCs, which need auxiliary circuits for forced commutation. However, these very high power applications are beyond the scope of this work, and the following discussion will therefore be concentrated on voltage-source converters.

Table 3.1: Soft-switching converters for motor drive applications.

	parallel	series
resonant AC link	 PRACL (parallel resonant AC link)	 SRACL (series resonant AC link)
resonant DC link	 PRDCL (parallel resonant DC link)	 SRDCL (series resonant DC link)
resonant pole	 ARCP (auxiliary resonant commutated pole)	

3.1.3.2 Resonant DC link converters

Parallel resonant DC link (PRDCL) converter

An equivalent circuit for the PRDCL converter [17] is shown in Fig. 3.4. The output section is modeled by a current source, based on the assumption that the load circuit has a high inductance and that the load current varies slowly with respect to the DC link frequency. Analysis of the circuit operation can begin by assuming that switch S_s remains open, that the load current is zero and that the DC link components are ideally lossless. Under these conditions, if the supply voltage is suddenly applied to the resonant tank, the voltage across the resonant capacitor C_r will oscillate sinusoidally between zero and twice the DC supply voltage. The DC link voltage would then exhibit periodically zero-voltage opportunities during which the power semiconductor devices at the output section could be switched on or off without switching losses. However, if the resonant tank is not lossless, the DC link voltage will never return to zero. The switch S_s is then included in the circuit to ensure that the resonant DC link voltage will always return to zero in order to produce a sustained DC link pulsation. Furthermore, switch S_s also ensures that the DC link voltage will remain at zero for a finite time interval, in order to provide enough time for commutation of the main output devices.

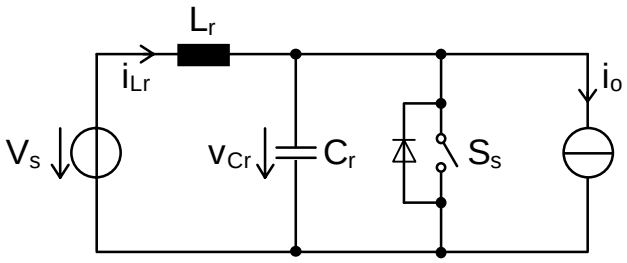


Fig. 3.4: Equivalent circuit for the PRDCL converter.

If S_s is kept closed while the supply voltage is applied, the current in the resonant inductor L_r will rise linearly. S_s should then be held closed until the magnetic energy stored in L_r ($0.5L_r i^2$) is enough to compensate for the losses in the

If the output section of the PRDCL converter is composed by half-bridge inverter legs as shown in Table 3.1, the function of switch S_s can be executed by the output switches themselves. In this case, S_s can be eliminated from the circuit. The converter circuit will be therefore very simple, having only two additional passive elements in comparison to a hard switched converter. No additional power semiconductor device is required. However, due to the pulsed DC link voltage, only discrete pulse modulation techniques can be used for output control. Furthermore, the higher voltage stress on the power semiconductor devices at the output section, in excess of 2 p.u. of the supply voltage, represents a major drawback of this topology. Several alternative topologies which limit the peak voltage stresses have been proposed to solve this problem [12, 18, 86]. So far, the most successful alternative topology is the actively-clamped resonant DC link converter [19], which is discussed next.

Actively-clamped resonant DC link (ACRDCL) converter

An equivalent circuit for the ACRDCL converter is shown in Fig. 3.6. The ACRDCL converter is obtained by augmenting the PRDCL converter with a clamping loop around the resonant inductor L_r. This clamping loop is composed by the clamping capacitor C_c and the clamp switch S_c, with its associated anti-parallel connected diode.

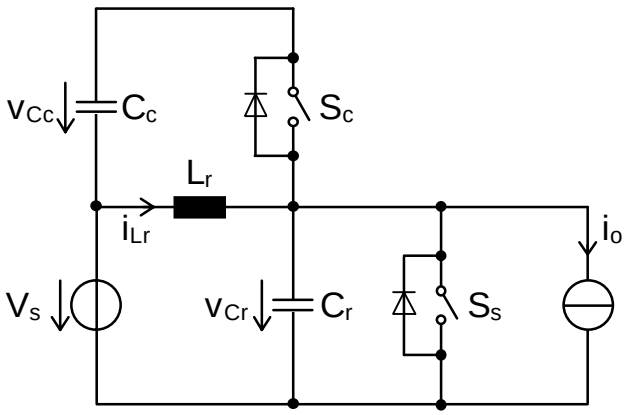


Fig. 3.6: Equivalent circuit for the ACRDCL converter.

The turn-off current reference I_c is supplied by a control loop which regulates the voltage across the clamping capacitor. If C_c is large enough, the voltage across it will exhibit only a small change during one clamping cycle. However, the control loop must ensure that the excess charge injected into C_c at the beginning of each clamping cycle is returned to the main circuit in finite time, with the objective of maintaining the long-term charge balance in C_c , thus keeping the clamp voltage stable. The total clamping voltage ($V_s + v_{Cc}$) can be approximately expressed as the supply voltage multiplied by a constant clamping factor k_c:

$$(V_s + v_{Cc}) = k_c \cdot V_s \quad , \tag{3.1}$$

and the voltage across the clamp capacitor is then given by:

$$v_{Cc} = (k_c - 1) \cdot V_s \quad . \tag{3.2}$$

This clamping factor k_c should be chosen according to the supply voltage and to the voltage rating of the power semiconductor devices employed. For example, with industry-standard power modules rated at 1200V and with a rectified AC voltage equal to 600V, a clamping factor of approximately 1.5 would be a good choice, yielding a maximum voltage stress of 900V.

The clamp switch S_c , as well as the shunt switch S_s , are turned off with low switching losses, under zero voltage conditions. This is achieved by the presence of the resonant capacitor C_r across the DC link, which slows down the voltage rise at the terminals of both switches when they cut off the current. As in the PRDCL converter, the intervals where the DC link voltage is zero are used for lossless commutation of the output switches, which distribute the DC link voltage pulses among the output phases. The function of the shunt switch S_s can be performed by the switches of the output section, if its topology allows shorting the DC bus. In this case, switch S_s is redundant and can be eliminated, rendering a converter with only one extra power semiconductor device in comparison to a conventional hard-switched converter. For this reason and due to the limited voltage stresses, it is claimed by several authors [22,

diagram with the equivalent circuit for the PRDCL converter, shown in Fig. 3.4, it can be recognized that both topologies are transmutable in each other if the current sources are replaced by voltage sources, parallel-connected capacitors by series-connected inductors and parallel-connected unidirectional blocking voltage switches by series-connected unidirectional current switches. The waveform of the current pulses in the SRDCL is also analogous to that of the voltage pulses in the PRDCL, shown in Fig. 3.5. Accordingly, the SRDCL will produce high current stresses in excess of twice the DC bias current I_d .

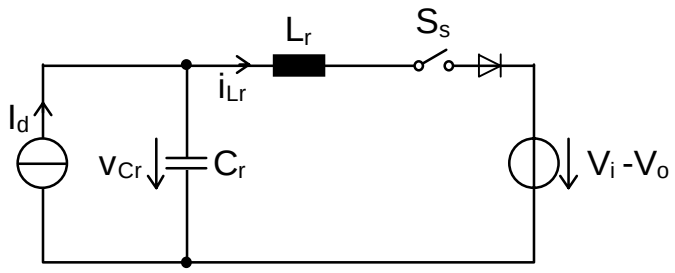


Fig. 3.9: Equivalent circuit for the SRDCL converter.

In [3], an interesting example of utilization of a SRDCL for a DC motor drive is shown, where the motor is connected in the same branch as the smoothing reactor. In this application there is no output converter, since the motor is directly supplied by the DC link. In AC applications, where an output converter is needed, the output has current source characteristics. For motor loads, capacitors must be parallel-connected at the output terminals in order to absorb the difference between the resonant current pulses and the motor input currents. This kind of drive system has usually slower dynamics than VSI drive systems, and are mostly not advantageous in low to medium power ranges.

On the other hand, resonant pole converters have the disadvantage of containing a considerably higher number of additional components, in comparison to other hard- and soft-switching converter topologies. Moreover, the resonant pole concept is not very suitable for application with output stage topologies other than half-bridge inverter phase legs. Consequently, most resonant pole topologies found in the literature cannot be directly applied to the SR converter configurations presented in section 2.3.

There is an alternative topology derived from the resonant pole concept, in which however the resonant transitions take place at the DC link. It is the auxiliary quasi-resonant DC link (AQRDCL) converter, and its equivalent circuit is shown in Fig. 3.11. The AQRDCL comprises only one resonant pole located in the DC link, and this pole is identical to the ones in the ARCP converter. All legs of the output section are connected between nodes *a* and *b*, and are shown in the circuit diagram of Fig. 3.11 for only one AC phase.

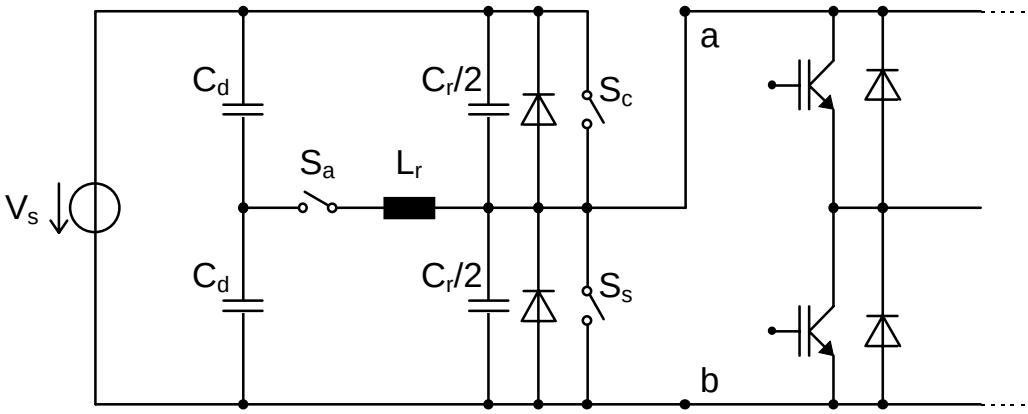


Fig. 3.11: Equivalent circuit for the AQRDCL converter.

In the AQRDCL, the DC link voltage does not oscillate continuously. When commutation of switches in the output section is needed, the resonant commutation circuit is triggered into conduction through the auxiliary switch S_a, producing a full swing of the DC link output voltage from V_s to zero, and back to V_s after a very brief shorting time. While the DC link is shorted, the switches at

found in the literature [15, 50, 71, 83, 101]. In the following sub-sections, the soft-switching SR converter topologies reported in the literature are discussed, as well as the applicability of the topologies presented in section 3.1.3 to SR drives.

3.2.1 ZCS C-dump converter

Le-Huy et al. [50] and Uematsu & Hoft [101] have proposed two very similar soft-switching SR converter topologies. Schematic diagrams for these circuits are shown in Fig. 3.12 (a) and (b), respectively. Both circuits consist of a modified C-dump converter, comprising fast thyristors as main switches. In both diagrams, the winding of one motor phase is represented by the inductor L_m. Auxiliary circuits including a resonant tank (formed by L_r and C_r) and an auxiliary switch (S_a) have been added for each phase, in order to achieve zero-current commutation of the main thyristor switches (S_m). However, the control of the voltage across the C-dump capacitor (C_c) is done by a hard-switched chopper in both circuits. This chopper comprises an inductor (L_c) and a semiconductor switch (S_c), which has been implemented with a bipolar transistor in [50] and with an IGBT in [101]. The number of additional components is also the same for both topologies, but the arrangement and the operation of the auxiliary circuits are different.

In the circuit (b), the main thyristors are operated as full-wave zero-current switches. The auxiliary thyristors provide free-wheeling paths for the phase current, allowing operation in soft-chopping mode. Phase current control is achieved through frequency modulation. In the circuit (a), the resonant oscillation is interrupted a half-cycle after turn-on of the main switch, and the full DC supply voltage can then be continuously applied to the phase winding for a controllable time. At the end of this period, the other half-cycle of the resonant transition is released by gating the auxiliary thyristor, in order to turn off the main switch at zero current. This control method allows the use of PWM to regulate the phase currents. However, soft-chopping is not possible in this circuit. Additionally, the direct connection of the main thyristors to the C-dump

3.2.2 Series-resonant SR converter

Park and Lipo [83] have proposed a series resonant converter for SR drives, also using zero-current commutated thyristors as main switches. A schematic diagram of this converter is shown in Fig. 3.13, for a 6/4 SR motor, having a three-phase power supply input. In this topology, the average voltage across the resonant capacitors C_r , i.e. the voltage applied to the phase windings, is controlled by the repetition rate of the resonant current pulses injected in each phase circuit. The phase currents, in turn, are regulated in a CRPWM fashion, by making the average voltage applied to the phase windings to jump back and forth between a positive and a negative value, in a kind of indirect bang-bang control. No free-wheeling path is provided for the phase currents, so the current control can be regarded as hard-chopped.

For the voltage control of a phase to work properly during the dwell period, the voltage across the respective resonant capacitor C_r must always be lower than the mean supply voltage at the beginning of each resonant cycle. This voltage difference ΔV is necessary to drive the resonant oscillation. Since the thyristor switches are connected as half-wave zero-current switches, each resonant current pulse will end after the first positive half-cycle. During one resonant pulse, the voltage across C_r , i.e. the phase voltage, rises from V_s - ΔV to V_s + ΔV. At the end of each resonant pulse, the thyristors turn off under zero current and the phase voltage must be brought back to V_s - ΔV . In this circuit, the motor phase current alone is relied upon to accomplish this task. As the motor phase inductances are much higher than the inductance of the resonant tank, the phase currents do not change significantly during one resonant cycle and can be regarded as constant. Therefore, the phase voltage will decay from V_s + ΔV to V_s - ΔV with a nearly constant slope, which will be proportional to the load current. The duration of this decay will also vary accordingly, and a new resonant pulse is triggered only at the end of this decay period. As a result, the switching frequency will be strongly coupled to the load current.

For operation with dwell overlap, the voltage across the offgoing phase must be regulated at -V_s , while the voltage across the ongoing phase must jump

in Fig. 3.14. However, the auxiliary switch itself is hard-switched. The authors propose the use of a power MOSFET as auxiliary switch, because of its low switching losses. The conduction losses in the resonant subcircuit are also kept low, because it is only activated for a short time, preceding the turn-on of the chopping switch. When S_a is turned on, assuming that C_r is initially discharged, the DC link voltage will rise, describing a resonant oscillation. The voltage would ideally overshoot the supply voltage by 100%, but the anti-parallel diode of switch *S* will clamp the DC voltage at the supply level V_s . Switch *S* can then be turned on under zero voltage, with low switching losses. After turn-on of *S*, switch S_a is turned off in hard-switching mode. When *S* is turned off, the resonant capacitor C_r will provide ZVS conditions, slowing down the fall of the DC link voltage. This fall time, however, will depend strongly on the motor phase currents.

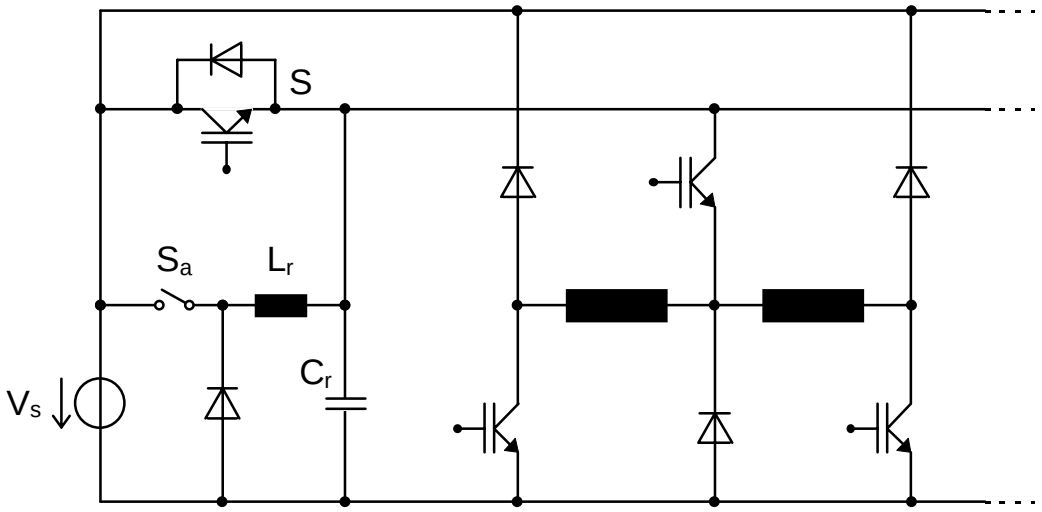


Fig. 3.14: ZVT PWM SR converter.

The use of voltage PWM to control the motor speed does not allow the achievement of the best attainable dynamic response. If the control is modified, this circuit is capable of realizing current-regulated PWM. However, the current overlap capability will be limited if the current control is realized through the switch *S* only. Independent current control can be realized if switch *S* is

the asymmetric half-bridge at the output section are connected directly to the supply rail instead of being connected to the quasi-resonant DC link.

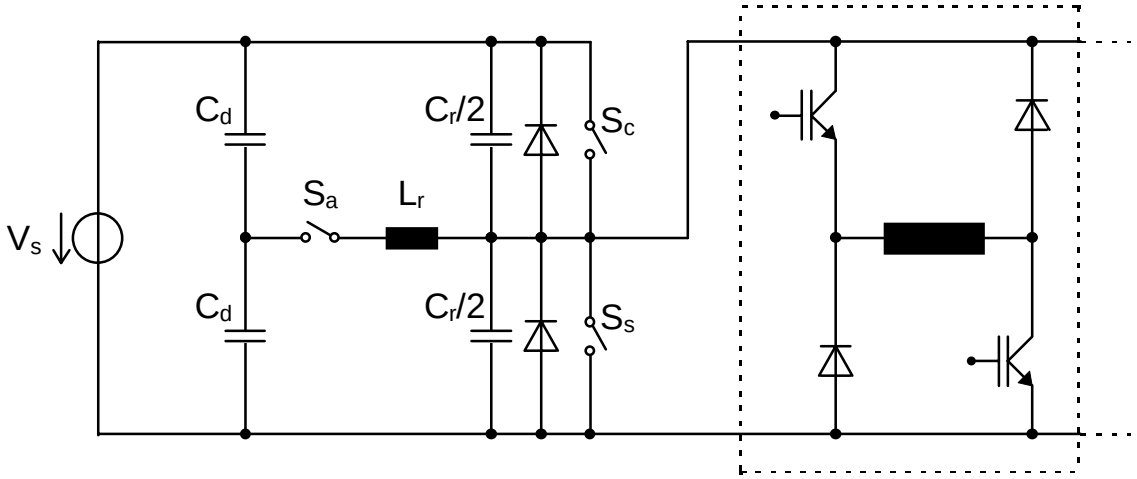


Fig. 3.15: AQRDCL SR converter.

3.2.5 Other topologies

Any of the topologies discussed in section 3.1.3 could in principle be easily adapted for application in a SR drive system, with exception of resonant pole converters, for the reasons already mentioned. However, some of those circuits would not suit very well to a high power density medium-power SR drive system. For example, resonant AC link circuits would be uneconomic due to the high number of bi-directional controllable power semiconductor devices required. According to Miller [60], the most suitable converters for SR drives are current-regulated voltage-source converters, because they permit operation at wide speed ranges. Therefore, SRDCL converters are also not appropriate, due to their current-source behaviour.

4 Technological Aspects

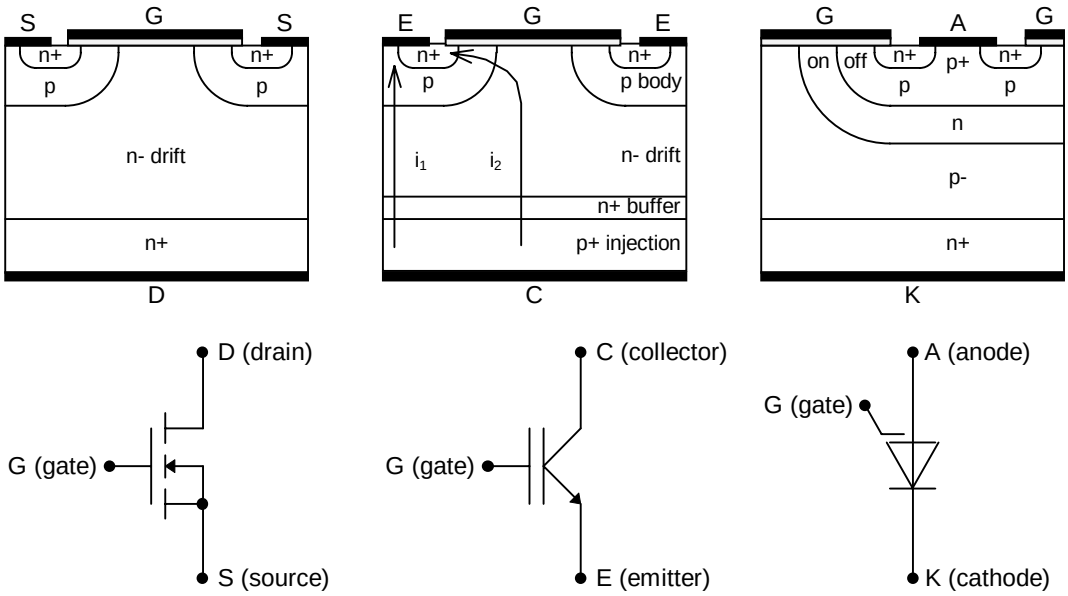
4.1 Power Semiconductors

The constant evolution of power semiconductor device technology is causing a progressive overlap of application areas for different devices. Devices with ever higher voltage and current ratings are being developed every year and this affects the choice of the most appropriate power semiconductor switches for new designs [33]. For electric drive applications, following controllable devices are presently commercially available:

SCR (Silicon Controlled Rectifier or Thyristor) - for very high power applications (>5 MW). Very high voltage blocking (>5 kV) and current conduction (>3 kA) capabilities. Has low switching speed and cannot be turned off from its control terminal (gate).

GTO (Gate Turn Off Thyristor) - for high power applications up to some MW. Voltage and current ratings comparable to SCRs. Switching speed is not very high, but depending on the power level it can switch, in hard commutation, at frequencies up to few kHz. There are publications showing that GTOs can switch at frequencies up to 20kHz if zero current switching is used. GTOs can be turned off from the gate, but the control current is relatively high and this is one drawback for low to medium power applications.

BJT (Bipolar Junction Transistor) - although many drive systems using these devices are still in operation, power bipolar transistors and power darlingtons are being gradually replaced by MOSFETs and IGBTs in new designs. Relatively high turn-off losses and turn-off delay, second breakdown and non-negligible power consumption at the control terminal are major disadvantages of this kind of device in comparison with its competitors.



(a) n-channel power MOSFET *(b) n-type PT IGBT* *(c) p-type MCT*

Fig. 4.1: Vertical cross-section of power semiconductor devices.

4.1.1 MOSFET

The power MOSFET is a so-called unipolar device, because only majority carriers take part in the conduction process. As a result, it exhibits a resistive behaviour in the on-state. If the doping level is increased and/or the thickness of the drain drift zone (Fig. 4.1 (a)) is decreased in order to achieve a lower on-state resistance, then the voltage blocking capability is reduced and vice-versa. For devices with voltage blocking capability above a few hundred volts, the dependence of on-state resistance on breakdown voltage is approximately given by

$$R_{on} \propto V_{BR}^{2.5-2.7}. \tag{4.1}$$

The practical consequence of this fact is the limitation of the current-carrying capability due to on-state power losses in devices with higher voltage ratings.

component is primarily responsible for the turn-off current tail. Component i_2 is a MOSFET-like current and thus drops very quickly at turn-off. The i_1 component, however, continues to flow as a current tail, until the excess minority carriers recombine in the drift region. In NPT IGBTs, which usually exhibit lower emitter efficiency, i_2 makes up most of the total device current (up to 90%). Hence, the current fall-time at turn-off is commonly lower for NPT IGBTs. In NPT structures, the carrier lifetime in the drift region is kept high in order to minimize conduction losses, but this also implies a lower recombination rate and a slower decay of the tail current. On the other hand, PT IGBTs have higher emitter efficiencies, leading to higher initial values of current tail. However, the n+ buffer layer is designed to have a much shorter carrier lifetime than the drift region, causing a faster decay of the tail current.

The overall effect of the switching mechanisms described above is a lower turn-off power loss for NPT IGBTs under hard-switching conditions. Nevertheless, this may be not true for soft-switching applications. Due to the longer current tail times exhibited by NPT IGBTs, they produce higher turn-off losses under zero-voltage soft-switching conditions than PT IGBTs [82]. The current turn-off process of NPT IGBTs seems not to work properly at reduced rates of change of collector-to-emitter voltage during turn-off as it occurs in ZVS circuits. Switching losses even higher than in the hard-switched case have been reported for NPT devices in a ZVS application [89]. In ZCS circuits, the turn-off behaviour of NPT IGBTs is not a problem, because the circuit itself provides for current zeroing before the power semiconductor device is switched off. In contrast to this, PT IGBTs are better suited for zero-voltage soft-switching operation, but the rate of reduction of switching losses depends strongly on the dv/dt at turn-off. Additionally, the maximum attainable switching frequency depends on the type of device optimization, discussed next.

In PT IGBTs, it is possible to modify the carrier lifetimes and the emitter efficiency of the BJT section, leading to different combinations of conduction and switching properties. Therefore, in PT IBGT chip design, a fundamental trade-off exists between switching speed (or switching energy) and on-state voltage drop, i.e., between switching losses and conduction losses. A typical graph of

Table 4.1: Typical switching losses for PT IGBTs of different generations

generation	***V_{CE} rating (V)***	***e_{on} (mJ/A)***	***e_{off} (mJ/A)***
2nd.	600	0.02–0.09	0.02–0.41
	1200	0.09–0.19	0.12–0.78
3rd.	600	0.03–0.06	0.03–0.07
	1200	0.12–0.20	0.12–0.15

4.1.3 MCT

The MOS-controlled thyristor (MCT) is composed of a very fine cell structure (down to a few μm cell size) of the type shown in Fig. 4.1 (c). It comprises separate "on" and "off" FET-like channels underneath the gate metallization, which are unevenly distributed along the surface of the silicon wafer (typically 1 turn-on channel for every 20 turn-off channels). The pnpn structure directly below the anode is the thyristor portion of the device. An equivalent circuit for the p-MCT is depicted in Fig. 4.3, showing the equivalent on- and off-FET structures, as well as the pair of positive-feedback connected transistors that represent the thyristor part. At turn-on, a negative voltage is applied between gate and anode, opening the on-FET channel while keeping the off-FET channel closed. This will initially enable current to flow through the on-FET into the base of the npn transistor in the thyristor pair, triggering the regenerative turn-on mechanism of the thyristor part and causing the device to latch on. Turn-off is accomplished by inverting the gate-source voltage, closing the on-FET channel while turning on the off-FET. The on-FET channel will then divert the collector current from the pnp transistor in the thyristor pair, breaking up the latch condition. The base current of the npn transistor in the thyristor pair is then interrupted, turning it off.

shorted out and the latch condition cannot be broken. However, the aforementioned shortcoming is not so much critical in SR drive applications, since the converter topology itself exhibits a very low potentiality for short-circuits. Additionally, the low on-state voltage drop and associated power losses is very important in some SR converter topologies, where two power switches are connected in series with the phase windings.

MCTs exhibit very good behaviour in soft-switching circuits [16, 77]. In zero-current soft-switching applications, switching losses can be almost completely eliminated, but the higher current stress will cause higher conduction losses. In addition, the limited turn-off capability of the MCT is of little significance in zero-current soft-switching circuits. With zero-voltage soft-switching, switching loss reduction over 50% can be achieved, provided the rise time of anode-cathode voltage at turn-off is longer than the tail current duration. In ZVS soft-switching application, switching losses are mainly dictated by turn-off. Turn-on losses are mostly negligibly small.

4.2 Passive Components

The choice of appropriate passive reactive components is very important for the successful design of a soft-switching converter. Due to the higher frequencies and the higher current stresses that normally occur in such converter topologies, the non-ideal inductors and capacitors in the circuit will dissipate non-negligible power. Therefore, these components have to be carefully chosen or designed, so that their power losses do not outweigh the switching loss savings on the power semiconductors. Conversely, some passive component technologies can lead to oversized parts in order to keep power losses below acceptable limits. Some guidelines for the choice of reactive elements for soft-switching circuits are given below.

imity effects. If the cross section of the winding conductor has to be large, for greater current carrying capacity, its smallest lateral dimension should not be larger than twice the skin depth of the material used, at the desired operating frequency. Otherwise, the current will concentrate near the surface of the conductor, resulting in a higher effective resistance and higher ohmic power losses. As an example, the skin depth in copper conductors is shown in Fig. 4.5 as a function of the operating frequency. In order to avoid losses caused by skin effect, one may have to use high-frequency Litz wires, with small, individually isolated conductor bundles. Other conductor arrangements suitable for high-current, high-frequency operation include flat braid wires and solid thin sheet conductors. Litz windings exhibit a very low copper fill factor (typically 30%), whilst fill factors better than 90% can be achieved with sheet conductors.

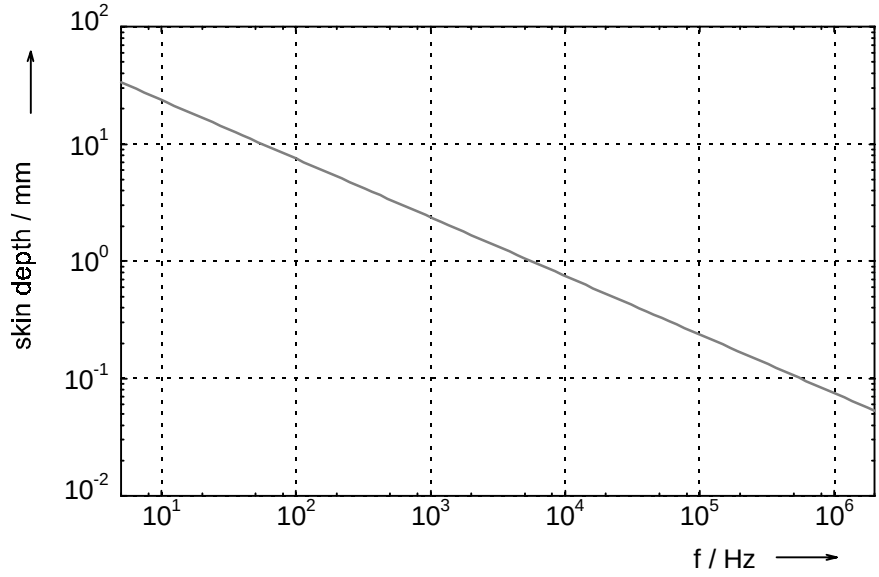


Fig. 4.5: Skin depth in copper ($\rho_{cu}=2.2\times10^{-8}\Omega\cdot m$ at $\theta=100°C$).

If a magnetic core inductor is used, the magnetic material should produce the lowest possible losses in the core. Low-loss ferrite cores are a good choice. Magnetic steel cores should be avoided, because they exhibit not only hysteresis losses, but also eddy current losses, which substantially increase total core

Electrolytics

Electrolytic capacitors exhibit moderate energy densities (< 1 kJ/kg) and high capacitance densities (reaching up to some tens of μF/g). However, their equivalent series resistance (ESR) is relatively high and the associated power losses will be also high for high ripple currents. Therefore, the actual capacitance to be used in a high ripple-current application must frequently be 10 to 100 times higher than the ideally required value, in order to obtain acceptable ESR losses and/or to satisfy the ripple current requirements. As a result, the actual capacitor size and weight in an electrolytic application may be considerably large. Electrolytic capacitors are best suitable for applications were very large capacitance values are required, but the frequency and the RMS value of the ripple current are low.

Film

Film capacitors have very low ESR and dissipation factor and are available for voltages up to several kV, independent of polarity. Due to the low ESR, the current ripple capability is usually very high, but the capacitance density is low. Hence, the reactive power density is high (> 50 kVA/kg) and the energy density is modest (> 0.1 kJ/kg). Film capacitors are well-suited for high-frequency, high peak current applications, where the required capacitance value is not so large, e.g. in snubber circuits. Film capacitors can also be successfully applied as resonant capacitors in soft-switching converters.

Ceramics

Ceramic capacitors exhibit lower energy density and lower capacitance density than electrolytic capacitors. However, the ESR and consequently the ripple current capability are high, yielding higher power densities than electrolytic capacitors. These properties can render more compact designs for capacitance values up to a few hundred μF. Larger capacitance value multilayer ceramic capacitors (MLC) are an emerging technology and are intended to replace electrolytic capacitors in some high-frequency, high ripple current applications. The use of MLCs in place of film capacitors in a resonant DC link converter has been also reported as advantageous [87]. However, the initial cost per μF of MLC capacitors is still considerably high in comparison to electrolytic or

5 Case Study: ACRDCL SR converter

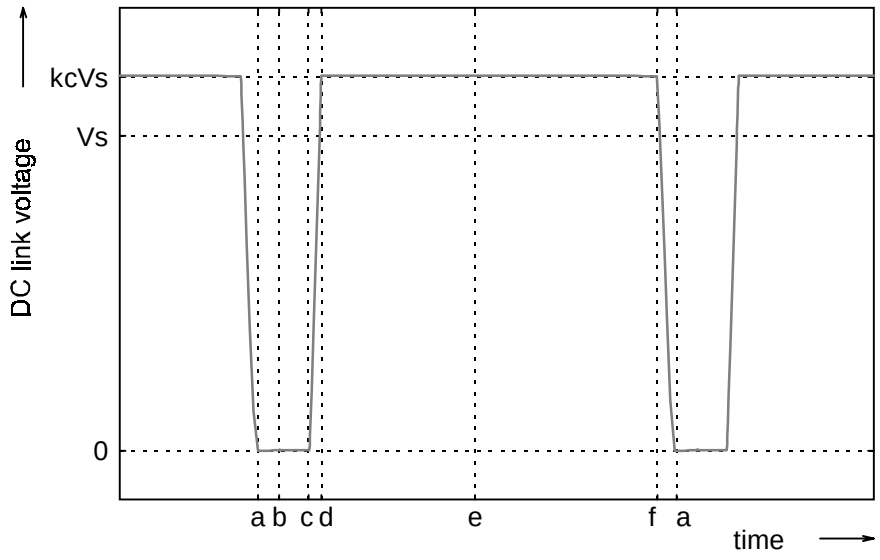
The operating principle of the actively clamped resonant DC link (ACRDCL) has been introduced in section 3.1.3. In this chapter, a detailed analysis of its operation is presented, including mathematical modeling, digital simulation and experimental evaluation. A modification of the basic ACRDCL is proposed for improved efficiency in combination with a SR drive. The interaction between the modified ACRDCL converter and a SR motor is investigated in detail, using as a model one of the prototype SR machines which has been designed at the Institute of Electrical Machines, University of Technology Berlin, within the scope of a BRITE-EURAM project [31]. The whole drive system has been simulated using the freely available circuit simulation program SPICE. The drive system has been tested in the laboratory, using a self-constructed converter controlled by a DSP control card installed in a personal computer.

5.1 Circuit Analysis of the ACRDCL

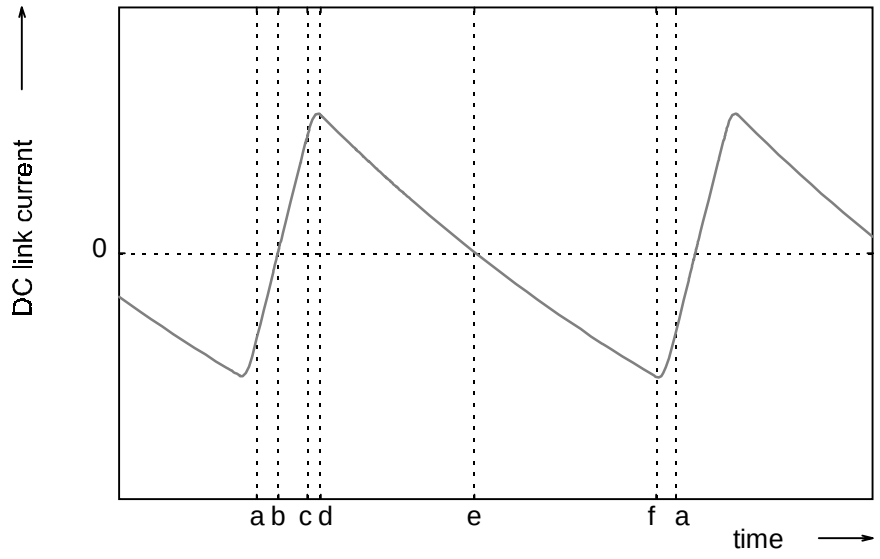
The currents and voltages of interest for the mathematical circuit analysis of the ACRDCL are shown in the schematic diagram of Fig. 5.1. All the circuit elements are assumed to be ideal, i.e., the switching times and the losses are considered negligible. The clamp capacitor C_c is assumed to be pre-charged to an initial voltage equal to $(k_c - 1)V_s$, where k_c is the clamping factor, defined in equation (3.1). The resonant tank in the DC link, formed by L_r and C_r, has the following characteristics:

natural frequency:
$$\omega_r = \frac{1}{\sqrt{L_r \cdot C_r}}, \quad f_r = \frac{\omega_r}{2\pi}; \tag{5.1}$$

characteristic impedance:
$$Z_r = \sqrt{\frac{L_r}{C_r}}. \tag{5.2}$$



(a)



(b)

Fig. 5.2: DC link voltage (a) and current (b).

The operating sequence of the ACRDCL can be split in four periods, which are described below, for the case of no-load operation.

boost period (from instant ***a*** to ***c***)

The branches that are active during the boost period are highlighted in Fig. 5.3. During the time interval between instants ***a*** and ***b*** (Fig. 5.3 (a)), the diode D_s

The initial value of the DC link current at the beginning of this interval is termed I_o . The variation of i_{Lr} during the boost period is given by:

$$i_{L_r}(t) = I_o + \frac{V_s}{L_r} \cdot (t - t_a). \tag{5.3}$$

The duration of the boost period is given by:

$$T_{boost} \cong \frac{(I_T - I_o) \cdot L_r}{V_s}. \tag{5.4}$$

rising resonant transition (from ***c*** to ***d***)

The active path during this period is shown in Fig. 5.4. At $t = t_c$, switch S_s is turned off and the link current is diverted into the resonant capacitor C_r . The initial current in C_r will be the "trip" current value I_T , which was flowing through S_s at the end of the boost period. The voltage v_{Cr} will then immediately start a rising oscillation toward its natural peak. This period ends when v_{Cr} reaches the clamping voltage level $k_c \cdot V_s$.

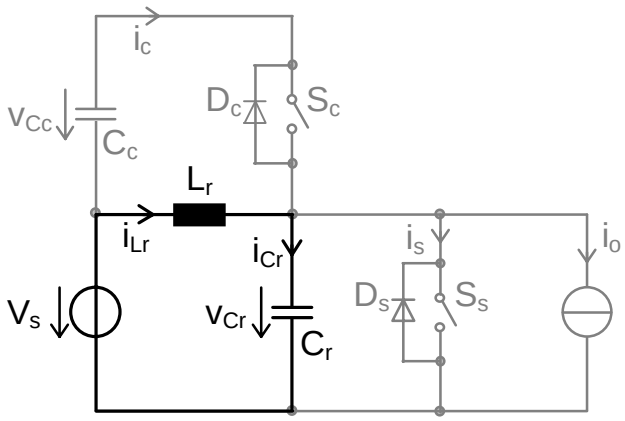


Fig. 5.4: Active path during the rising resonant transition.

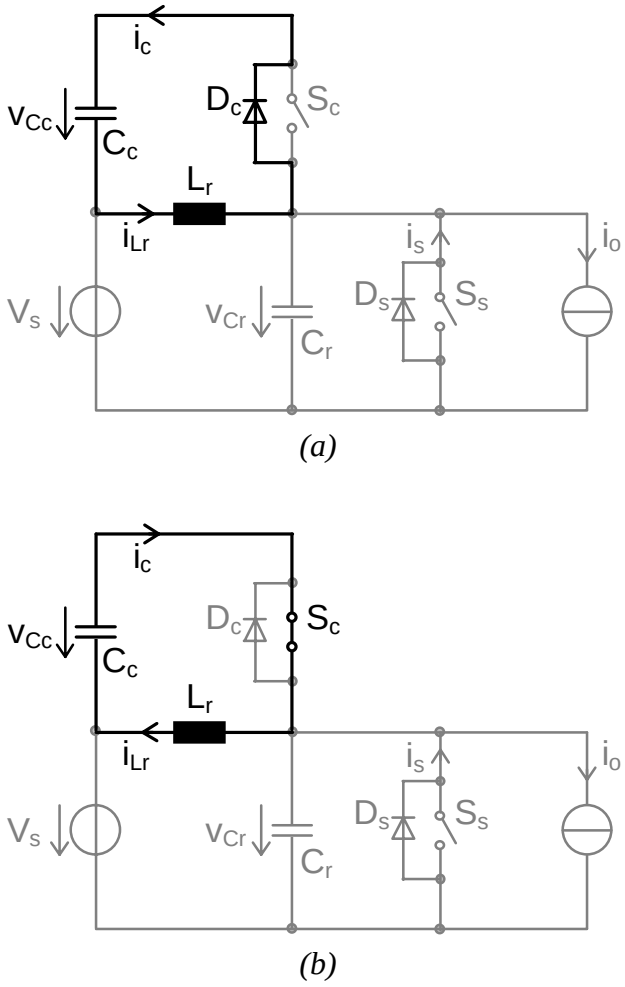


Fig. 5.5: Active paths during the clamp period
*(a) between instants **d** and **e***
*(b) between instants **e** and **f***

The current magnitude at the beginning of the clamping process can be obtained by substituting (5.7) into (5.6), and is given by:

$$|I_{co}| = \sqrt{I_T^2 + k_c(2 - k_c)\left(\frac{V_s}{Z_r}\right)^2} \,. \tag{5.8}$$

The voltage and the current on the clamp capacitor can be written as:

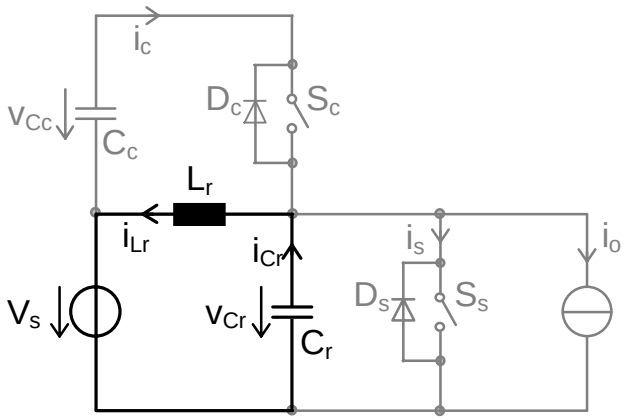


Fig. 5.6: Active path during the falling resonant transition.

The link voltage and current during this period can be written as:

$$v_{C_r}(t) = V_s - \sqrt{(k_c - 1)^2 V_s^2 + Z_r^2 I_c^2}\, sin\left[\omega_r (t - t_f) + tan^{-1}\left(-\frac{(k_c - 1)V_s}{Z_r |I_c|}\right)\right]; \quad (5.14)$$

$$i_{L_r}(t) = \sqrt{I_c^2 + \frac{(k_c - 1)^2 V_s^2}{Z_r^2}}\, sin\left[\omega_r (t - t_f) + tan^{-1}\left(\frac{Z_r |I_c|}{(k_c - 1)V_s}\right)\right]. \quad (5.15)$$

The duration of the falling resonant transition is given by:

$$T_{fall} = \frac{1}{\omega_r}\left[sin^{-1}\left(\frac{1}{\sqrt{(k_c - 1)^2 + \left(\frac{Z_r I_c}{V_s}\right)^2}}\right) - tan^{-1}\left(-\frac{(k_c - 1)V_s}{Z_r I_c}\right)\right]. \quad (5.16)$$

The link current at the end of the falling resonant transition is given by:

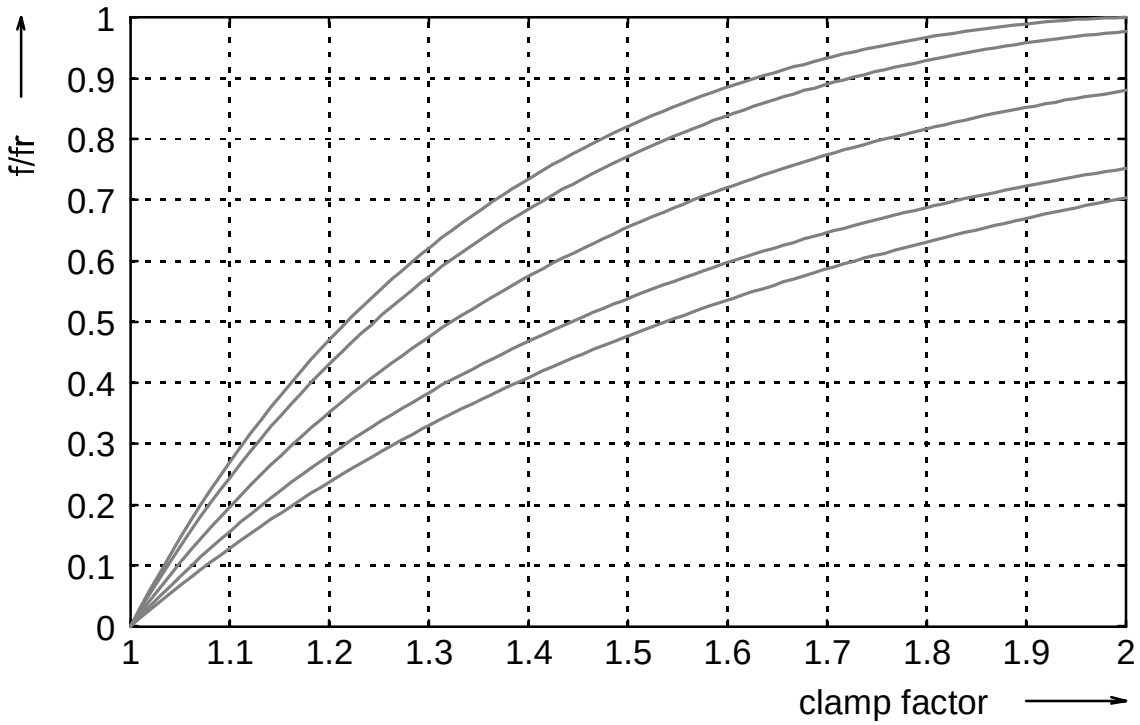


Fig. 5.7: No-load link frequency (in p.u. of the resonant frequency) versus clamp factor for k_b varying from 0 (upper trace) to 2 (lower trace) in 0.5 steps.

clamp voltage control

To maintain the clamp voltage regulated, the net charge transferred to the clamp capacitor C_c must be zero. This can be achieved by actuating upon either the trip current value I_T for the boost period or the turn-off current value I_c for the clamp period. Closed-loop control of v_c can be done using a PI controller, for instance. In this work, I_c has been selected as actuating variable, while I_T is kept constant. However, I_c should not fall below a lower limit, to ensure that the resonant tank will have sufficient energy to resonate the DC link voltage down to zero. An upper limit should also be set, for overcurrent protection. If a PI controller is used with this kind of saturable actuating signal, it is important to implement some anti-windup strategy, to avoid excessive oscillation of the clamp voltage in the event saturation occurs. A block schematic of the clamp voltage control loop with anti-windup is shown in Fig. 5.8.

ance of the resonant tank, as well as for the capacitance of the clamp capacitor. The choice of settings for the clamp factor k_c , for the trip current I_T at the end of the boost period and for the trip current I_c at the end of the clamp period also influences strongly the overall performance of the circuit and should be carefully done. Some hints for the choice of these parameters have been presented in [17, 18], for ACRDCL induction motor drives. Here, a detailed discussion of design criteria is presented, intended for the design of ACRDCL converters for SRM drives.

choice of natural frequency

For an effective reduction of the switching losses in the main switches, the transition time of the DC link voltage during the rising resonant period (T_{rise}) should be considerably larger than the current fall time of the power semiconductor devices employed (T_f). This will set an upper limit for the natural frequency of the resonant tank, according to equation (5.7). At this point, it is useful to introduce a "relief factor", defined as $k_r = \frac{T_{rise}}{T_f}$. This factor is a rough measure of how much a particular power semiconductor device, with its characteristic switching times, is being relieved from the switching stress. Based on the above definition, the natural frequency of the resonant tank in the ACRDCL should then be chosen as:

$$f_r < \frac{1}{2\pi \cdot k_r \cdot T_f}\left[sin^{-1}\left(\frac{(k_c - 1)}{\sqrt{1 + k_b^2}}\right) - tan^{-1}\left(-\frac{1}{k_b}\right)\right] \tag{5.23}$$

Assuming, for example, a current fall time of T_f = 500ns for the power semiconductors, a clamp factor of k_c = 1.5, a boost factor of k_b = 1.0 and a relief factor of k_r = 3 , it can be obtained from (5.7) that the natural frequency f_r should be no greater than ca. 120kHz. Under the above conditions, it would result in a maximum obtainable clamped DC link frequency of nearly 78kHz.

choice of characteristic impedance

The characteristic impedance of the resonant tank should be chosen so that the overall converter losses are minimized. At a first glance, an increase in DC link

and output behaviour. This results in a peak value for the resonant current in the DC link approximately equal to the peak value of the output current.

choice of resonant inductance and resonant capacitance

Provided the natural frequency and the characteristic impedance of the resonant tank have been chosen, the required inductance and capacitance can be calculated by solving equations (5.1) and (5.2) for L_r and C_r , yielding:

$$C_r = \frac{1}{\omega_r Z_r} \tag{5.26}$$

$$L_r = \frac{Z_r}{\omega_r} \tag{5.27}$$

choice of clamp capacitance

If the clamp capacitor is very large in comparison to the resonant capacitor, then the voltage across it will change very little during the clamping process in one cycle. This kind of clamp is then termed "hard clamp". In this case, the control of the clamp voltage can be done by a slow control loop, with a bandwidth well below the DC link frequency. The clamp voltage is then regulated by means of an energy balance over several periods of the DC link pulsation. For lower values of clamp capacitance, on the other hand, the clamp voltage can vary considerably during one cycle. For this kind of clamp, which is called "soft clamp", the control of the clamp voltage must be done in a per-cycle basis, resetting the clamp voltage at the end of each clamp period to its initial value. This requires a different type of control. If the losses are neglected, the voltage across the clamp capacitor during the clamping process, for no-load operation, is given by (5.9). The maximum variation of the clamp capacitor voltage can then be found by equating the time derivative of (5.9) to zero, solving for *t* and substituting it back in (5.9):

$$\Delta v_{C_c\,max} = \sqrt{(k_c - 1)^2 V_s^2 + Z_r'^2 I_{co}^2} - (k_c - 1)V_s . \tag{5.28}$$

5.3 Modified ACRDCL SR converter

A basic implementation of an ACRDCL SR converter has been presented in section 3.2.5. However, in the circuit shown in Fig. 3.16, the direction of the DC link current reverses if the phase current commutation is realized without dwell overlap. This behaviour leads to undesirable fluctuations of the DC link frequency, as has been shown in [89]. In order to avoid these current jumps in the DC link, the basic ACRDCL SR converter circuit can be modified by connecting the upper diodes of each phase leg directly to the clamp rail, as shown in Fig. 5.10. This modification provides at the same time a higher turn-off voltage for demagnetization of the phase windings, with the positive effect that has been illustrated in Fig. 2.16. In this configuration, however, the output stage should not be operated continuously in hard-chopped mode, since the lower phase leg switches do not commutate under ZVS conditions. However, if the phase current control is realized by soft chopping with the upper switches, their switching losses will be considerably reduced.

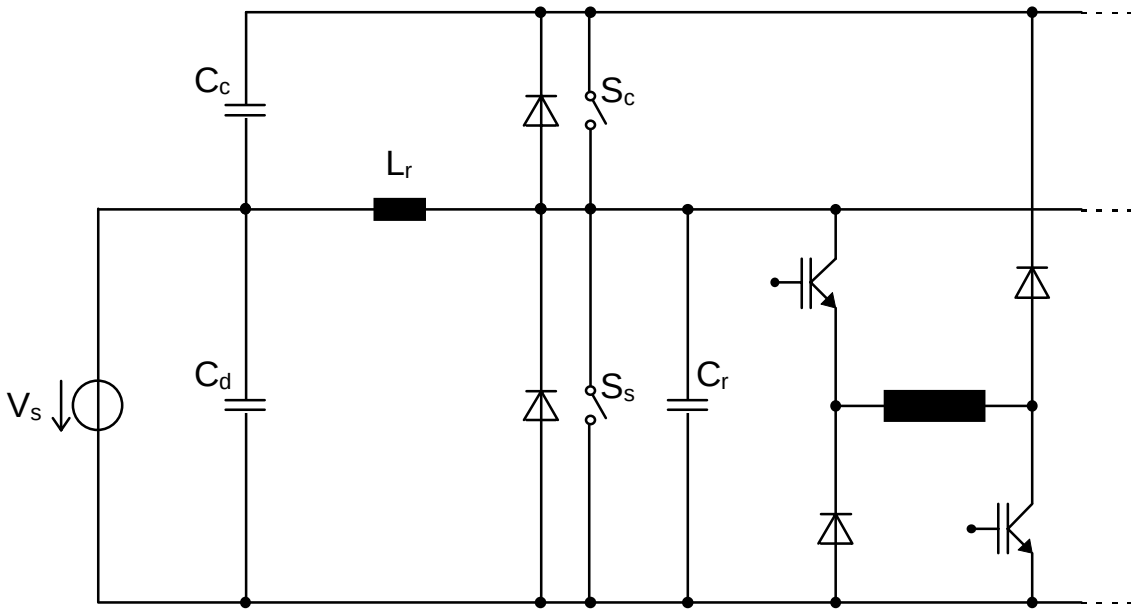


Fig. 5.10: Modified ACRDCL SR converter.

scribed using SPICE's built-in non-linear controlled sources [84]. As an example, the calculation of the counter emf of one phase is described below.
The tabulated magnetization data consists on a set of triplets (i_j , θ_k , $\psi_{j,k}$), which are obtained from field calculations or from direct measurements. The aimed interpolated output from the subcircuit can be then mathematically described by:

$$\psi(\theta,i)=\sum_k \frac{ramp(\theta-\theta_k)-ramp(\theta-\theta_{k-1})}{\theta_k-\theta_{k-1}}\cdot(y_k-y_{k-1}), \tag{5.31}$$

where:

$$ramp(x)=\frac{x+|x|}{2} \tag{5.32}$$

and

$$y_k=\sum_j \frac{ramp(i-i_j)-ramp(i-i_{j-1})}{i_j-i_{j-1}}\cdot(\psi_{j,k}-\psi_{j-1,k}). \tag{5.33}$$

Each term y_k can be then represented by j controlled current sources connected to a node k, where they are summed up. The resulting subcircuit output, in turn, is formed by summing up, at an output node, the k contributions comprised in (5.31). The desired counter emf is obtained by letting the output current flow through an one-henry inductor. The voltage across this inductor is fed back in the phase circuit through a unity-gain controlled voltage source, as shown in Fig. 5.11.

frequency electromechanical transients for a complete drive system would be impractical with such accurate switch models, due to the long computing times involved. Parameter extraction is also rather cumbersome for accurate models, and simulation results for a specific device cannot be readily generalized for other device types.

Several simulations have been carried out using the model of the BRITE-EURAM prototype SR machine. The purpose of the simulations has been:

- to investigate the influence of the clamp voltage on the phase demagnetization and on the torque production,
- to choose optimum commutation angles,
- to choose appropriate values for the control system parameters.

5.4.1 Prototype SRM data

The motor used in the experiments has the per-phase static torque and flux linkage characteristics shown in Fig. 5.12 and in Fig. 5.13, respectively. More details of the motor design can be taken from Appendix I. The torque measurements have been done for currents between 0.5A and 5.0A, in 0.5A steps, with five-degree interval between measured positions. Position 0 corresponds to the aligned position. The flux linkage characteristics are also shown with five-degree intervals. The flux linkage characteristics have been obtained indirectly, by integrating the motor's voltage equation (2.10). Current and voltage have been digitally measured with blocked rotor, for several rotor positions, and the voltage equation has been numerically integrated. Detailed descriptions of this methodology and other measurement methods can be found in [11, 41, 56, 60]. The static torque has been measured directly with an inductive torque transducer mounted on the shaft and blocked at one side.

5.4.2 Influence of the clamp voltage

It has been mentioned in section 2.4.1 that the torque production of the SRM can be improved, if the demagnetizing voltage at turn-off is higher than the supply voltage. In the modified ACRDCL SR drive system, the demagnetizing voltage is equal to the clamp voltage, so the torque production is directly affected by the clamp voltage level. The influence of the clamp voltage on the torque production of the prototype SRM has been investigated, by computing the absolute mean torque and the specific mean torque (Nm per ampere RMS) produced by one phase. The computations have been carried out for a supply voltage of 300V, constant speed of 1500 rpm, fixed turn-on angle of -45° and turn-off angles varying between -15° and 0°, in 1° steps. Two different cases have been compared and the results are shown in Fig. 5.14 (absolute torque) and Fig. 5.15 (specific torque). In the first case, the motor is fed from a conventional SR converter, with a resulting demagnetizing voltage equal to the supply voltage. In the second case, the motor is fed from a modified ACRDCL SR converter (Fig. 5.10), with a clamp factor of 1.5 and with a correspondingly higher demagnetizing voltage. In both cases, the motor is operated in single-pulse mode. From the diagrams of Fig. 5.14 and Fig. 5.15, it can be seen that the turn-off angle for which the maximum torque production occurs, shifts toward the aligned position when the demagnetizing voltage is higher. Additionally, the maximum achievable absolute torque increases by approximately 4% and the maximum specific torque increases by ca. 3% when the turn-off voltage is 50% higher than the supply voltage. The specific torque per phase current is directly related to the efficiency of the energy conversion process, so an equivalent gain in machine efficiency can be expected if it is fed from a modified ACRDCL converter.

5.4.3 Choice of optimum commutation angles

The commutation angles influence the torque production in many different ways. On the one hand, higher average torque and lower torque ripple can be attained if the machine operates with appreciable dwell overlap. Control of the current shape during overlap can then reduce the torque ripple to very low values [93]. On the other hand, the total average torque produced per phase RMS amperes can get lower at large overlap angles. So, the machine efficiency is also expected to reduce under these conditions. Unfortunately, the maximum average torque, the maximum efficiency, the minimum torque ripple and the minimum noise do not occur for the same set of commutation angles. Moreover, the values of turn-on and turn-off angles that optimize the above quantities depend also on the reference current level, on the turn-on and turn-off voltages and on the speed. As a result, the determination of an optimum set of commutation angles is not easy and requires the definition of an optimization criterion specific for the wanted application.

In this study, the commutation angles that maximize the total average torque per phase RMS current, and consequently also the machine efficiency, have been searched. It has been assumed that the machine is required to operate at full load torque, for three speed ranges (low, medium and high). The optimum commutation angles have been determined by simulating the modified ACRDCL SR drive system in the steady-state, supplied from a 300V voltage source and with a clamp factor of 1.5. The current reference value for full load torque has been set to approximately 5A, and the speed values which characterize the low, medium and high speed ranges have been set to 500 rpm, 1000 rpm and 1500 rpm, respectively. The optimum turn-off angle for each speed has been first searched for a fixed turn-on angle of -45°. The optimum turn-off angle was then searched, while the optimum turn-off angle found previously was maintained. Simulation results showing the variation of the torque with the commutation angles are presented in figures Fig. 5.16 to Fig. 5.19.

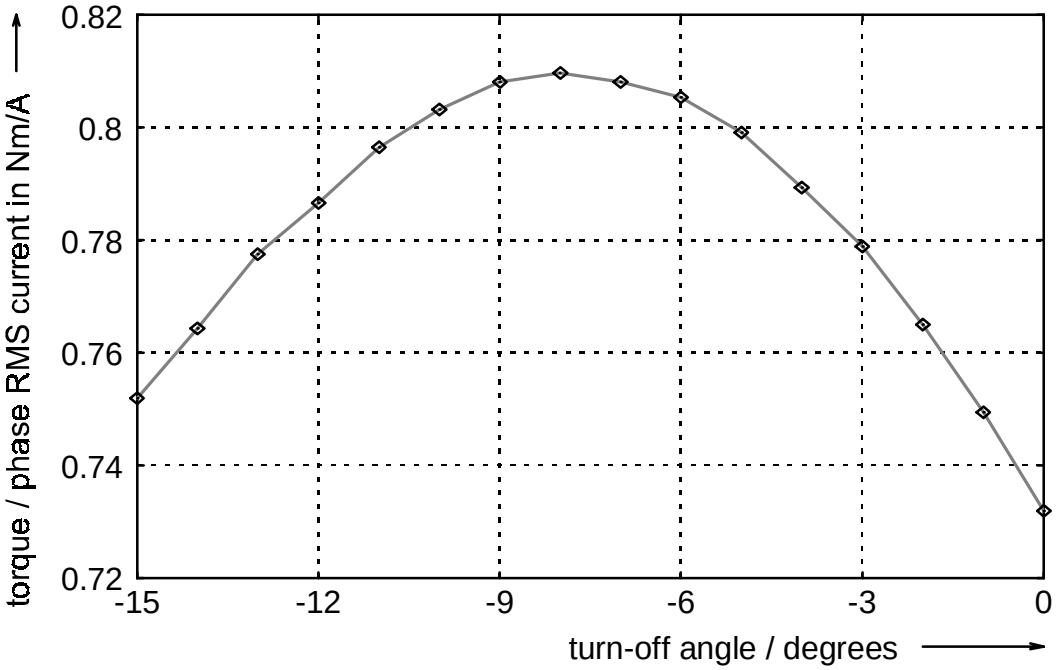


Fig. 5.18: Torque per phase RMS current versus turn-off angle at 1000rpm, for fixed turn-on angle (-45°) and for constant current reference (5A) (simulation results).

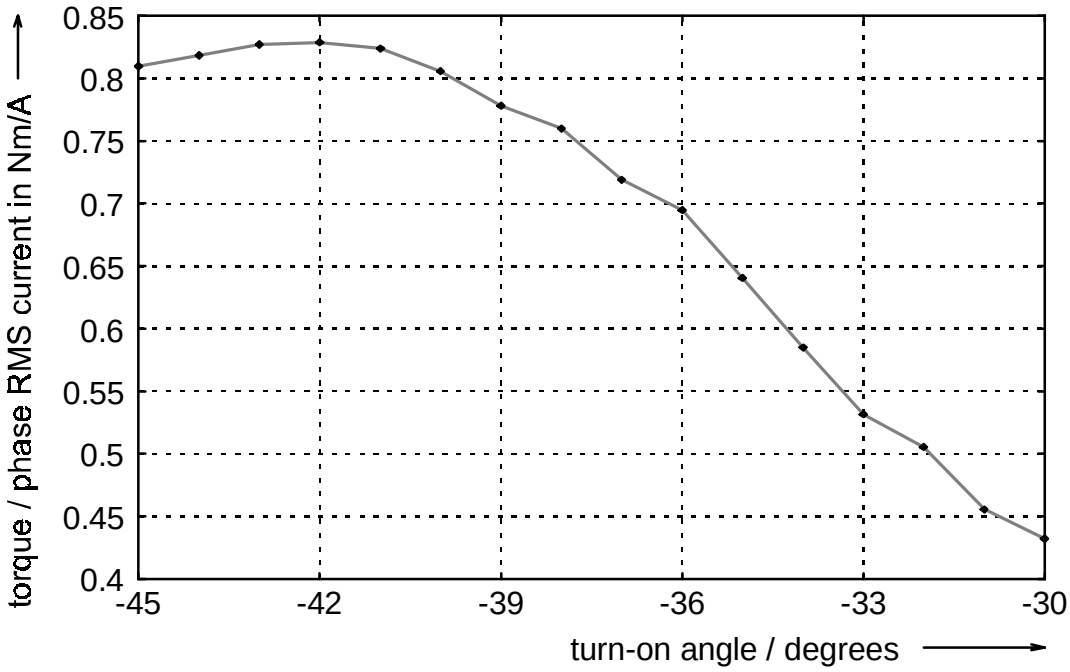


Fig. 5.19: Torque per phase RMS current versus turn-on angle at 1000rpm, for optimum turn-off angle (-8°) and for constant current reference (5A) (simulation results).

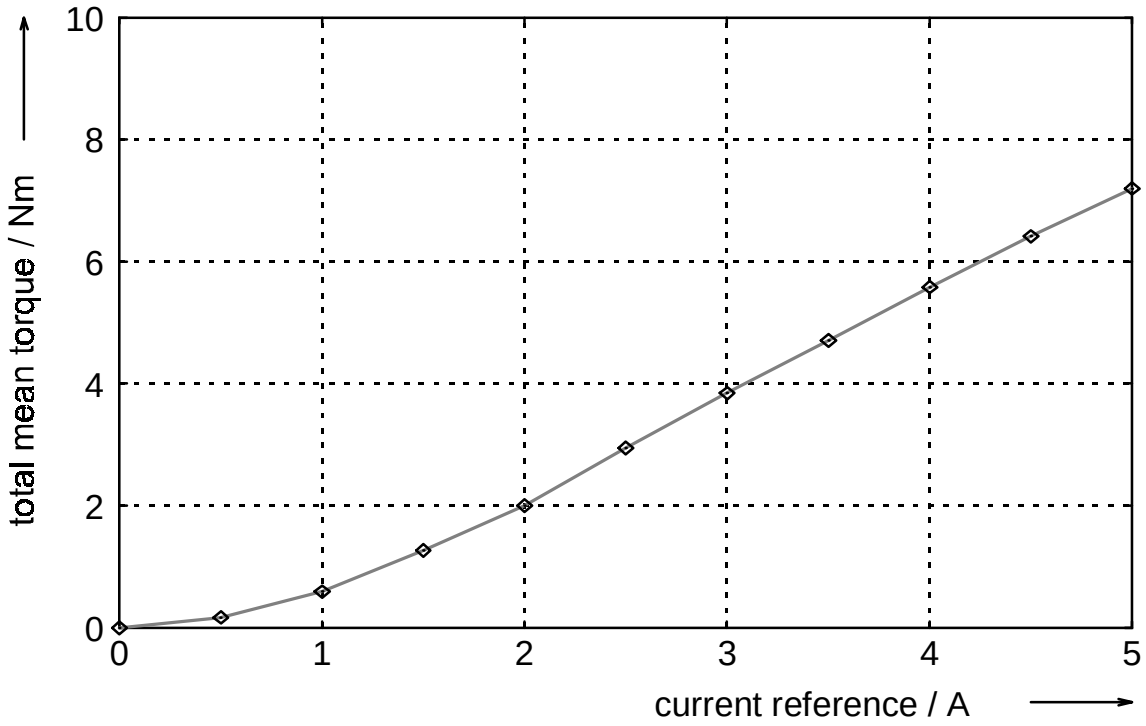


Fig. 5.21: Total mean torque versus current reference for current-controlled (chopped) operation at 1000 rpm (simulation results).

5.4.4 Control system parameters

For the choice of the control system parameter values, some worst-case simulations have been carried out. For the clamp circuit, the most critical situation is the braking operation, where additional energy is injected in the clamp capacitor every time a phase is commutated. Thus, the clamp control system must respond fast enough to prevent an excessive increase of the clamp voltage under this condition. On the other hand, a balance should be struck for the bandwidth of the clamp voltage control loop, if it is to be implemented digitally. The clamp control should not be too fast, in order to avoid an overburdening of the digital controller by too high a sample rate, but it should be fast enough to allow the use of a small clamp capacitor. The component values used in the simulations are:

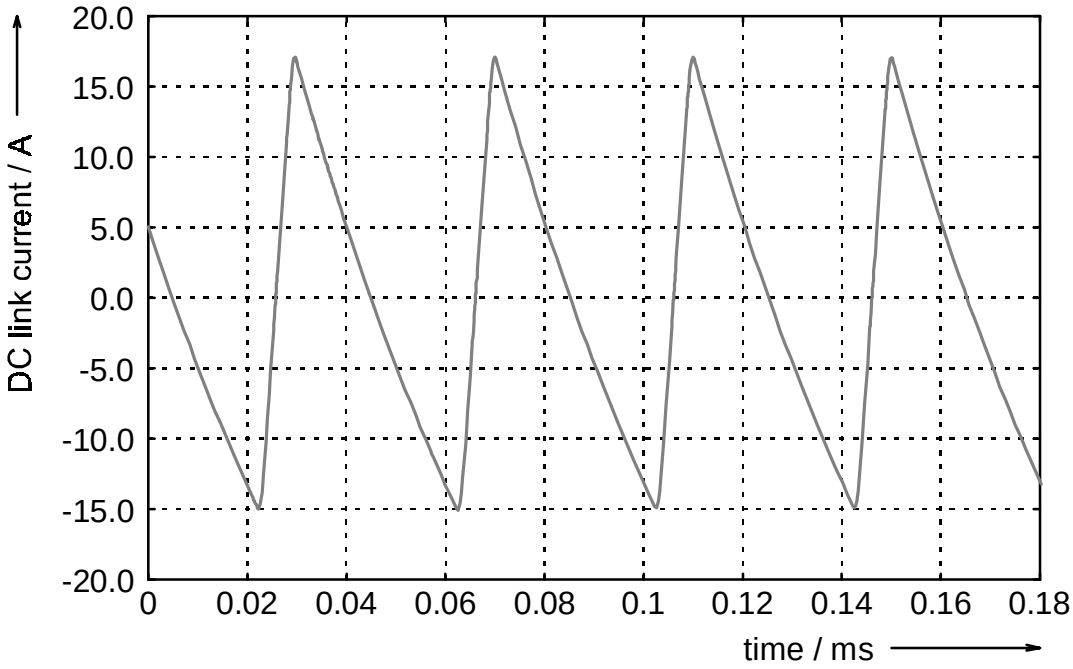


Fig. 5.23: Current throguh the resonant inductor (simulation result).

The clamp control system parameters have been set based on equation (5.22), after choosing the damping factor and the undamped natural frequency of the control loop. The response of the clamp voltage to the current injection from the phase windings during regeneration is shown in Fig. 5.24, with a mean value of 1A for the regenerated current.

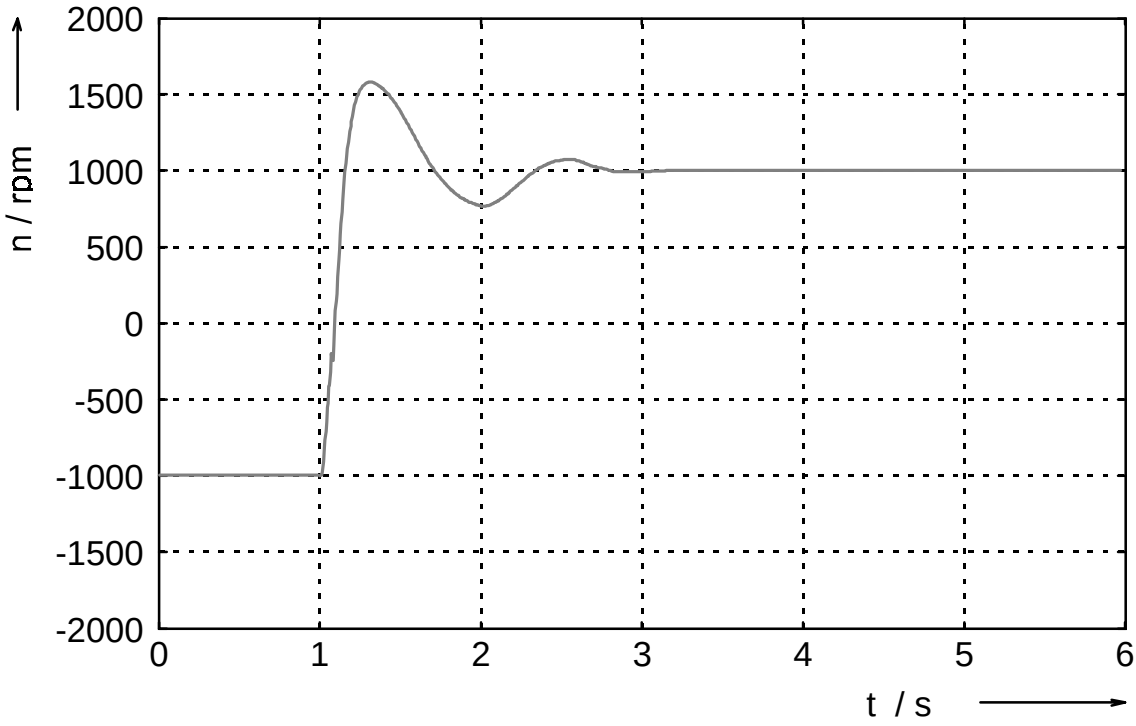


Fig. 5.25: Simulated motor response to reversal of speed reference signal.

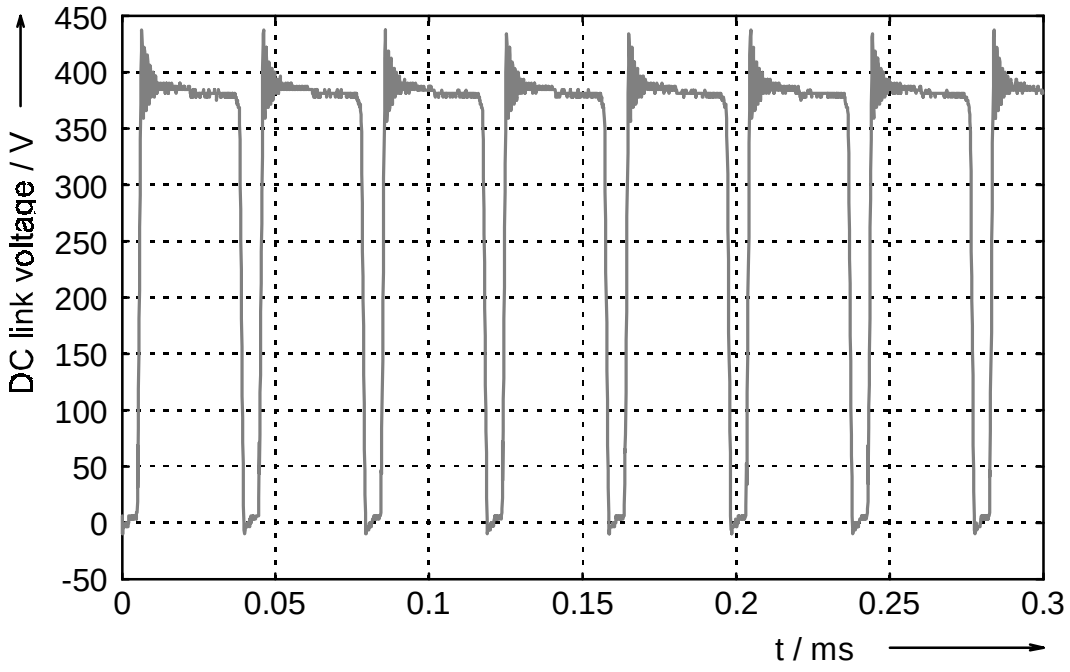
5.5 Experimental Assessment

In order to verify experimentally the validity of the results obtained from the simulations, an actively-clamped resonant DC link SR drive system has been constructed. The system comprises a 1.1 kW, 1500 rpm, 6/4 SR motor and a breadboard converter, controlled by a personal computer equipped with a DS1101 interface card. The DS1101 is a control card for motion control applications, made by dSpace GmbH. It is based on the TMS320C14 digital signal processor (DSP), from Texas Instruments Inc., and contains some useful peripherals for motion control, like analog I/O and incremental position encoder interfaces. The TMS320C14 itself is a fixed-point DSP with microcontroller characteristics and also has some on-chip peripherals, like timers/counters, event manager and PWM generator. It is capable of running at approximately 6.25 million instructions per second (MIPS), allowing the implementation of many control functions by software. A schematic diagram of the experimental test set-up is shown in Fig. 5.26.

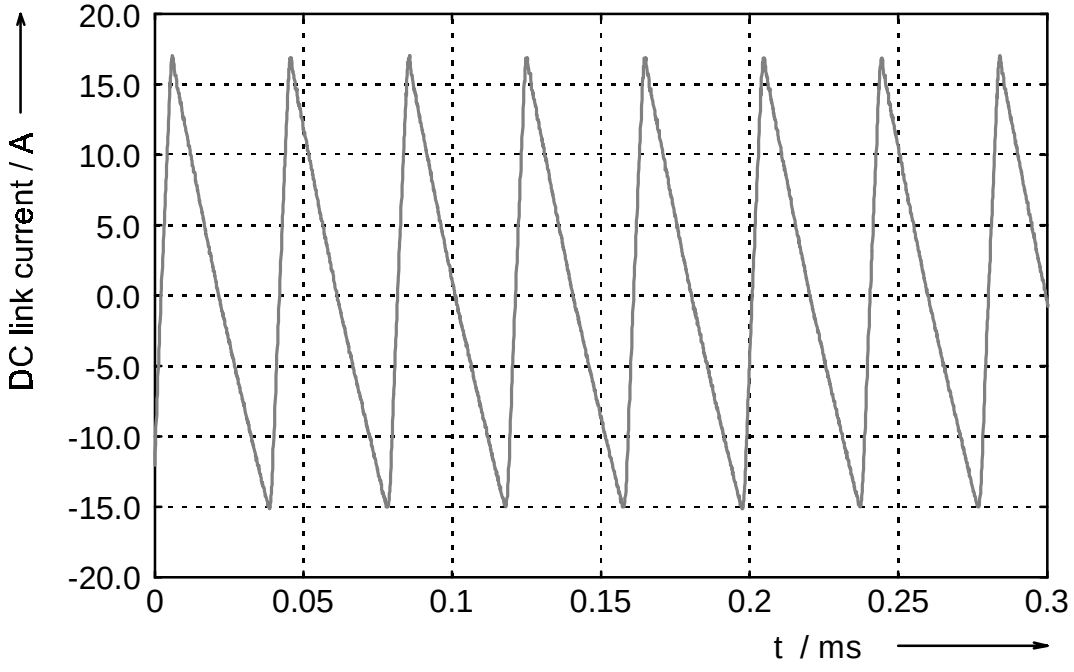
current control and supervisory protection are executed by an interrupt service routine which runs at the highest achievable repetition rate. Other functions like clamp voltage regulation and speed control are executed at lower repetition rates, but synchronized by the main interrupt routine. The implementation of a fast commutation algorithm is very important for the overall performance of the SR drive system. In this experimental setup, a fast phase commutation has been implemented by means of a fixed table of switch patterns. The table has 256 positions and covers 1/4 of a rotor revolution. The incremental position encoder also delivers 256 pulses per 1/4 of revolution, so that the table exactly matches the encoder resolution. For any entry in the commutation table, six bits (e.g. the 6 LSBs) are used to describe the state of the six switches in the output section, depending on the rotor position.

The tabulated switch patterns are computed off-line, so that the state bits of any phase are high when the rotor lies between $-\theta_d/2$ and $+\theta_d/2$ with respect to the aligned position for that phase, where θ_d is the dwell angle. The incremental encoder interface delivers a 16-bit word describing the rotor position. To this word is then added an offset of $\pm\theta_d/2$, depending on the sign of the product between the actual speed and the reference torque. This provides the displacement of the current pulse into the positive or into the negative torque-producing region, depending on the sense of rotation. Then, a commutation advance angle (speed-dependent optimum turn-off angle) is added or subtracted, depending on the sign of the actual speed (sense of rotation). At last, the 8 LSBs of the resulting word are used as an offset to read a switch pattern from the commutation table. This commutation algorithm is very fast, taking only a few instruction cycles to execute. At the highest sample rate achievable with the DSP controller, the maximum deviation from the calculated commutation angles at nominal speed is less than 0.4°.

As mentioned above, the sign of the torque produced by the SRM is determined by the commutation algorithm, by advancing or delaying the phase current pulses with respect to the aligned position, depending on the sense of rotation. Hence, the current regulation algorithm has to control only the magnitude of the phase currents. In this experiment, a simplified phase current con-



(a)



(b)

Fig. 5.27: Measured resonant DC link voltage (a) and current throguh the resonant inductor (b).

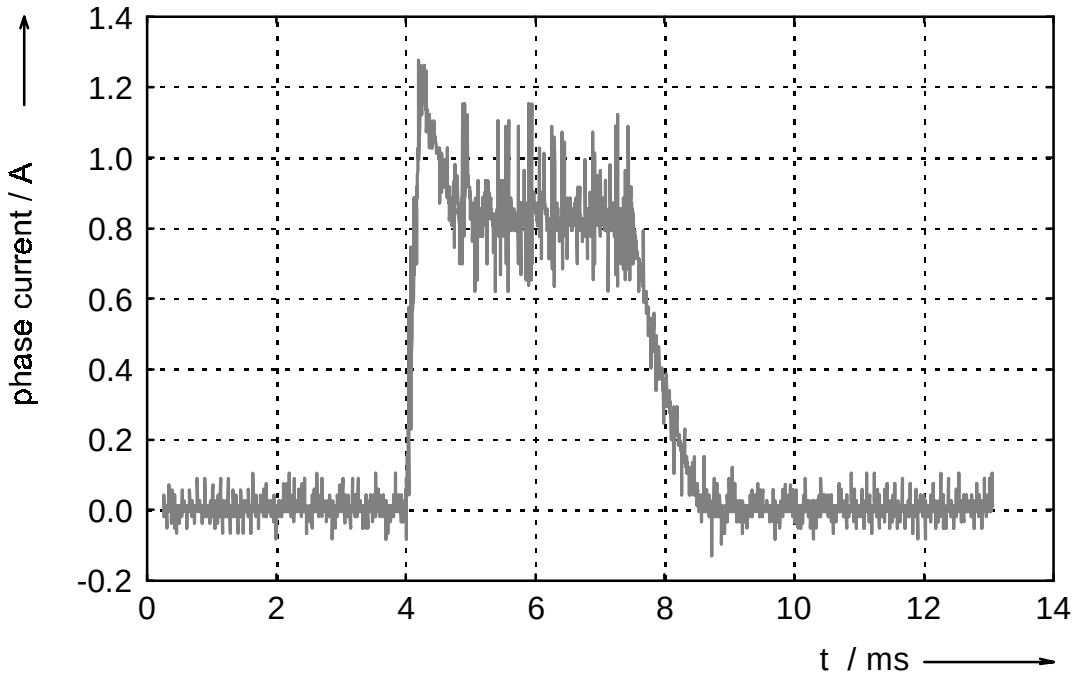


Fig. 5.29: Phase current for current-regulated operation at 1500 rpm.

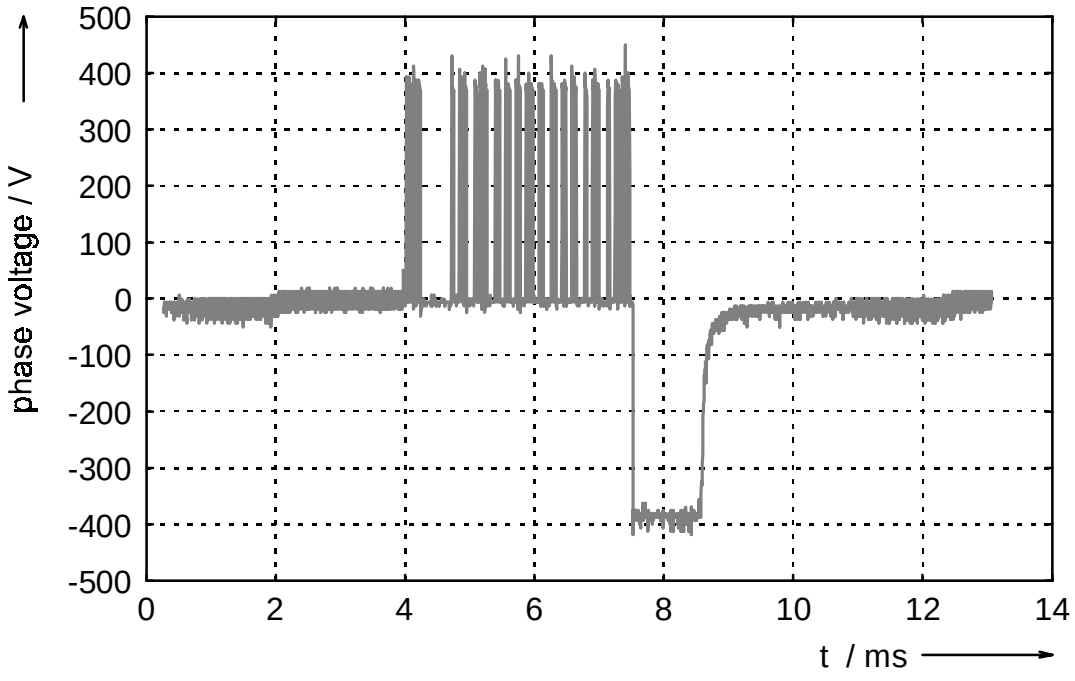


Fig. 5.30: Phase voltage for current-regulated operation at 1500 rpm.

Fig. 5.31 shows a speed reversal from -1000 rpm to +1000 rpm and back. The load has been chosen as purely inertial, in order to evidence the braking capa-

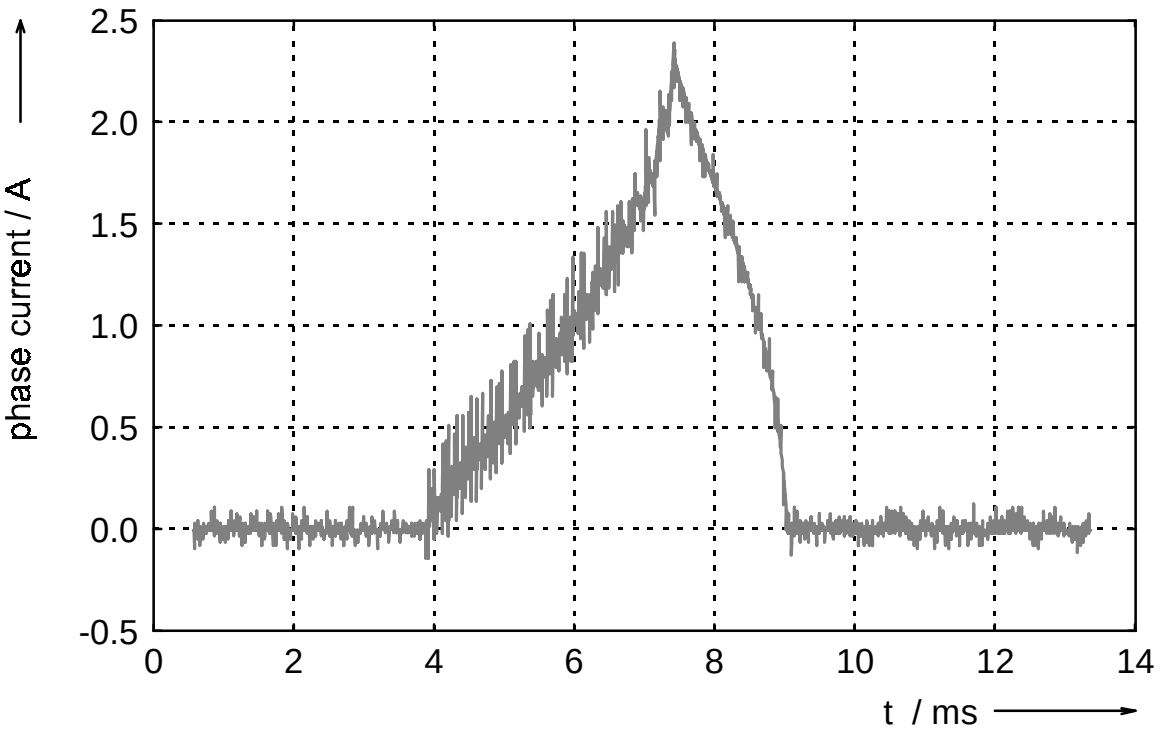


Fig. 5.32: Phase current for regenerative braking at 1500 rpm.

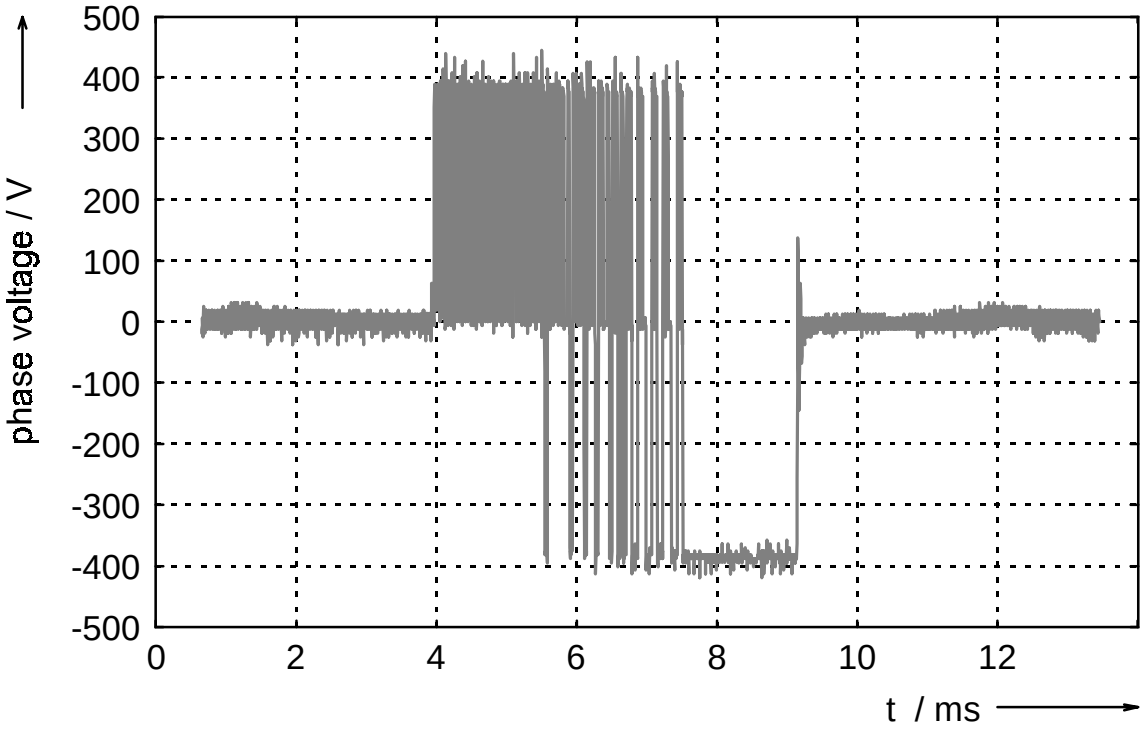


Fig. 5.33: Phase voltage for regenerative braking at 1500 rpm.

switched SR converter is thus also not possible. With the MCTs used, the converter could be operated at a much higher output power. However, the circuit has not been thermally and mechanically designed for such high powers. An extrapolation of the power loss measurements indicates that better efficiency could be achieved if the ACRDCL SR converter were operated at higher output power levels.

6 Discussion

In the previous chapter, a simulation model has been developed for the modified ACRDCL SR converter. The simulation model has been then experimentally validated for a low-power (1.1 kW, 1500 rpm) prototype SRM drive system. In this chapter, the simulation model which has been experimentally validated in chapter 5 is extrapolated for drive systems of higher power. A discussion on the efficiency, quality and power density of medium-power SRM drive systems is then presented.

6.1 Some considerations about efficiency

At first sight, it may appear that the most significant advantage of a soft-switched SR drive system would be an increase in efficiency, resulting from the quasi elimination of switching losses. However, from an economical point of view, the capital cost of a soft-switched SR drive system specifically developed for increased efficiency would be perhaps only payable by the energy savings at very high power levels. For example, in an application such as a heavy locomotive for goods transport (e.g. the E152 from the Deutsche Bundesbahn, 6.4 MW), an increase of the overall drive efficiency by 1% (say, from 90% to 91%), considering operation at 85% of the rated power on average, for 5000 working hours per year, would result in energy savings of round 50.000,– DM per year (at 0,15 DM/kWh). These savings would perhaps justify the investments, but the SRM is not the most appropriate motor for applications at these power levels, mainly due to following reasons:

- the torque pulsations of the SRM at such high torque levels could provoke premature fatigue failure of the shaft. The torque pulsations can be reduced by proper design and current control, but in this case the efficiency would be impaired;

Based on the above data, it can be said that the average switching frequency of the main output devices in an ACRDCL converter can be up to six times higher than the mean switching frequency of a conventional hard-switched PWM converter, without increasing the total power losses in the main semiconductor devices. However, the losses in the clamp circuit and in the resonant inductor of the ACRDCL must be taken into account if the overall losses of both converters are to be compared. So, the ratio between the average switching frequencies of the ACRDCL converter and of the PWM converter should be somewhat lower than six, for comparable overall losses. Experimental evaluations [21] have shown that the overall losses in a three-phase ACRDCL inverter are comparable to the overall losses in a conventional three-phase PWM inverter, if the DC link frequency of the ACRDCL converter is approximately ten times higher than the switching frequency of the PWM converter.

In the ACRDCL converter, control of the phase currents must be realized by discrete-time control methods, e.g. current-regulated delta modulation. If the sampling instants for the current control are synchronized with the zero-voltage notches of the DC link voltage, then the average switching frequency of the output switches will be strongly dependent on the DC link frequency, because the sample rate of the digital current control will be equal to the DC link frequency in this case. The average switching frequency depends also on other factors such as the supply voltage, the phase inductances and on the machine counter-emf, which in turn depends on the machine speed. In order to study the influence of the sampling frequency on the average switching frequency and on the power losses, a 11 kW hard-switched SR drive system with delta-modulated current control has been simulated. The simulations have been carried out for a supply voltage of 500V, constant speed of 1500 rpm, constant current reference of 40 A and sampling frequencies ranging from 20 kHz to 100 kHz. The simulation results are summarized in Table 6.1, showing a value of 0.3 for the ratio between the average switching frequency and the sampling frequency.

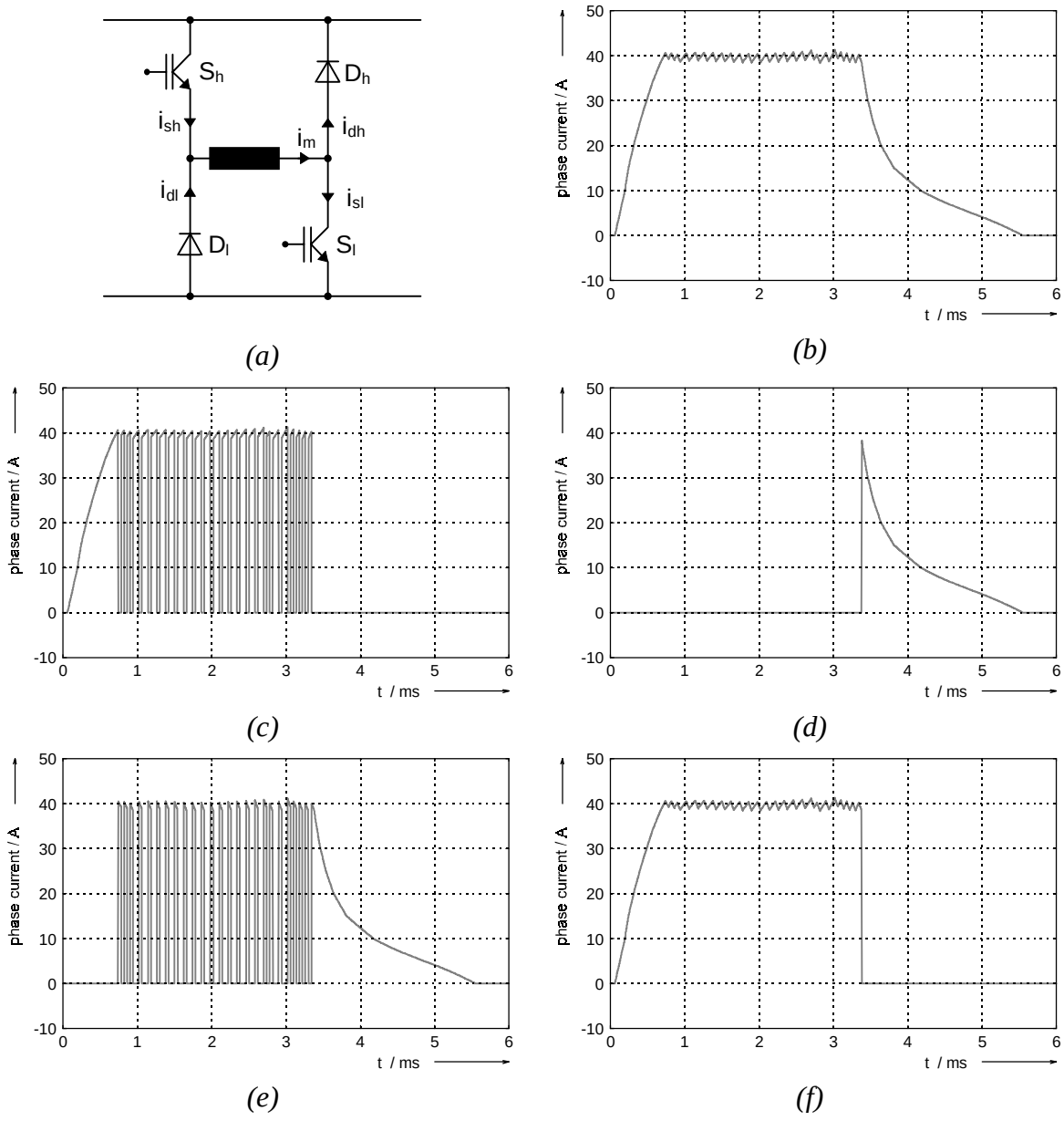
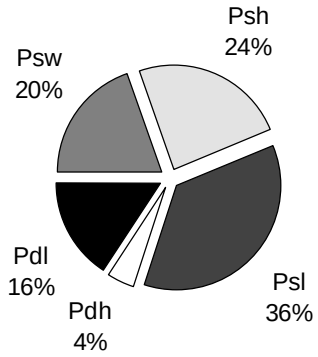
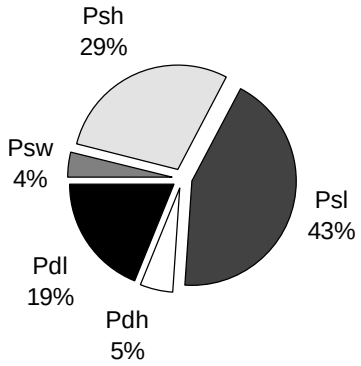
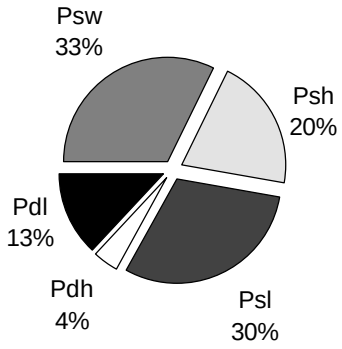
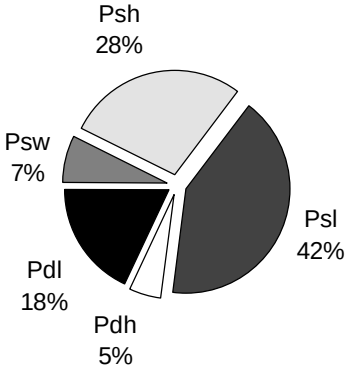
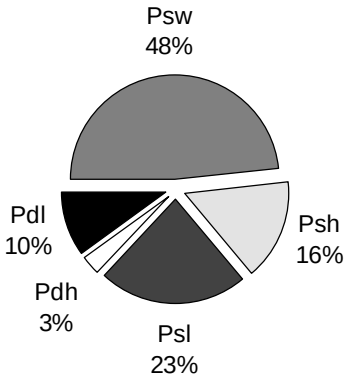
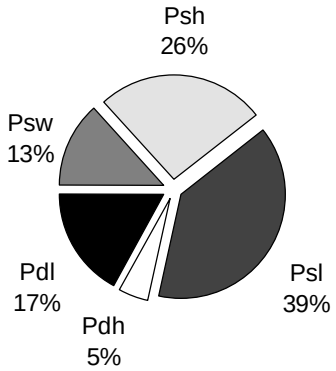


Fig. 6.1: Current throguh the components of an asymmetric bridge converter: (a) identification of the current components; (b) current i_m; (c) current i_{sh}; (d) current i_{dh}; (e) current i_{dl}; (f) current i_{sl} (supply voltage =500V, speed = 1500 rpm).

Table 6.2: Loss distribution in asymmetric bridge converter.

$\overline{f}_{sw}$(kHz)	*hard switching*	*soft switching*
7.5	 100% = 137.2 W	 100% = 114.7 W
15	 100% = 164.5 W	 100% = 120.3 W
30	 100% = 215.7 W	 100% = 129.0 W

has been calculated for each of the operating conditions shown in Table 6.1. The calculations have been carried out under the following assumptions:

- two semiconductor device configurations have been considered:
  - discrete, TO-247 packaged diodes and IGBTs;
  - industry-standard power modules;
- the thermal resistance of the components are the following:

R_θ	*TO-247*	*module*
junction to case (IGBT):	0.64 K/W	0.28 K/W
junction to case (diode):	0.83 K/W	0.38 K/W
case to heat sink (both):	0.24 K/W	0.10 K/W

- a temperature limit of 100°C has been set for the junction temperature of each component, and the ambient temperature has been assumed to be 50°C.

The calculated thermal resistances are shown in Table 6.3.

Table 6.3: Required thermal resistance in K/W from heat sink to ambient ($R_{\theta sa}$) for different values of mean switching frequency.

f_s	$\overline{f}_{sw}$(kHz)	*hard switching (TO-247)*	*soft switching (TO-247)*	*hard switching (module)*	*soft switching (module)*
20	6	0.0034	0.0196	0.0739	0.0924
25	7.5	-0.0070	0.0185	0.0667	0.0913
40	12	-0.0366	0.0169	0.0466	0.0881
50	15	-0.0531	0.0166	0.0355	0.0866
100	30	-0.1099	0.0134	-0.0025	0.0798

From Table 6.3, it can be seen that it is not possible to operate the hard-switching converter at a switching frequency of 7.5 kHz and above, if single

example, for instance, the power semiconductor modules would have a total weight of 900g, and a suitable heat sink for the hard-switching converter switching at 15 kHz would have a weight of approximately 5 kg. On the other hand, it would be possible to operate the soft-switching converter at a mean switching frequency above 20 kHz, using a smaller heat sink than the one that would be required to operate the hard-switching converter at a mean switching frequency of 6 kHz. In this case, although there would be practically no gain in power density, there would be a substantial quality gain if soft-switching were used, because quiet converter operation would be achieved.

Another important aspect related to the thermal alleviation produced by the use of soft switching is the reliability of the power semiconductor devices. In the example given above, even if the switching frequency of the soft-switching converter is raised by a factor of two with respect to the hard-switching converter, it is still possible to operate the power semiconductor devices at lower junction temperatures. This would reduce the failure rate, increasing the reliability of the converter (typically, the failure rate for semiconductor devices reduces by 50% for each 10-15°C temperature reduction from the maximum recommended junction temperature [67]).

The losses in the resonant DC link have not been computed in Table 6.2, but they have a significant influence on the final size of the ACRDCL converter. The DC link losses for a given natural frequency are strongly dependent on the characteristic impedance of the resonant tank. The main loss components in the DC link are the semiconductor losses in the clamp switch and in the shunt switch and the losses in the resonant inductor. The semiconductor losses have been computed for different values of characteristic impedance and are shown in Fig. 6.2. It can be seen that higher values of characteristic impedance produce lower semiconductor losses, because the circulating current in the DC link is lower. Moreover, the RMS current throguh the clamp capacitor will also be lower, allowing the use of a capacitor with smaller current rating (see discussion in section 4.2.2).

of two will require a fourfold increase of the number of turns. The winding resistance will also be four times higher, but the peak current will be halved, so that the ohmic losses caused by the resonant current will be roughly constant. However, the higher winding resistance will cause higher ohmic losses due to the load current. A better way of increasing the inductance and therefore the characteristic impedance of the resonant tank could be the use of a magnetic core of higher permeance on the resonant inductor. In this case, the winding resistance would not increase as much as in the previous case, and the ohmic losses would be lower.

The possibility of snubberless operation of the power semiconductor devices has been often pointed out as one of the advantages of soft-switching circuits. In ACRDCL converters, the absence of snubber circuits would counterbalance the extra volume added by the resonant tank and by the clamp circuit. In opposition to this idea, it has been claimed [73] that last-generation power semiconductor devices do not need to use snubber circuits to keep the devices' switching trajectories within the safe operating area (switching SOA), for hard-switching operation. However, it may be necessary to use snubber circuits or output filters in a hard-switched converter, in order to keep the rate of change (dv/dt) of the output voltage under acceptable values. According to the IEC 34-17, the rate of change of motor supply voltages must be lower than 500V/μs. Latest IGBT devices exhibit typical rise and fall times shorter than 1μs, so it is easy to exceed the IEC maximum dv/dt recommendations for circuits with DC supply voltages higher than 500V. Additionally, the displacement current in the winding insulation, which is caused by the high dv/dt, can produce high currents through the insulation to earth, especially near the winding terminals. If these current surges occur at a high repetition rate, the degradation of the insulation may be accelerated. Improper operation of protection circuits can also be provoked by these currents to ground. The switching frequency in a hard-switched converter may therefore have to be limited to avoid these problems.

In the ACRDCL SR converter, the dv/dt at the DC link voltage transitions does not depend on the switching characteristics of the power semiconductor de-

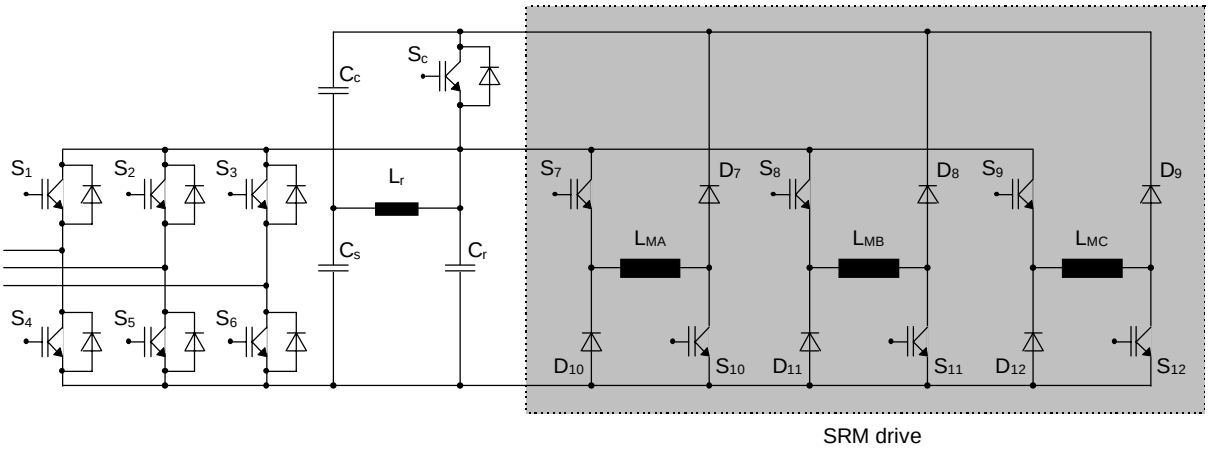


Fig. 6.3: ACRDCL SR converter with active rectifier in the input stage.

6.4 Conclusions

Based on the discussion presented in this section, it can be stated that the power density or the quality of a SRM drive can be considerably enhanced by using a modified ACRDCL converter. A considerable power loss reduction can be achieved if the soft-switching converter is operated in delta-modulation current control mode, in comparison to a hard-switching converter operating at the same switching frequency and with the same current control mode. For this reason, the use of soft-switching in SRM drives is more advantageous if the converter is operated in current-controlled mode most of the time. Operation in single-pulse mode at higher speeds is also possible with the ACRDCL SR converter, but in this case no significant loss reduction would be verified.

7 Summary and suggestions for further work

In this work, drive systems comprising switched reluctance machines and soft-switching converters have been investigated. Several hard- and soft-switching converter topologies have been studied and a suitable soft-switching converter topology for use in SRM drives has been analyzed with more detail. It has been pointed out that the proposed soft-switching SRM drive is capable of operation in current-controlled mode, with switching frequencies above the audible region, with better efficiency and higher power density than a hard-switching SRM drive.

The converter topology used in the proposed SRM drive system is a variation of the "actively clamped resonant DC link converter" (ACRDCL), which is considered by several authors as the most successful soft-switching converter topology for induction motor drives. A very simple modification has been introduced, which allows for applying a higher voltage on the phase windings during demagnetization when the phase current is commutated (turned-off). A simulation model for the proposed SRM drive system has been developed and the ratio between mean torque and RMS current has been evaluated for several different operating conditions. Also, the commutation angles that maximize the specific torque of the investigated machine for different operating conditions have been determined. In order to validate the simulation model experimentally, a breadboard DSP-controlled ACRDCL SR converter has been built.

It has been found out from the simulations that, despite the simplicity of the proposed modification in the SRM drive circuit, it enables a gain of about 3% in the specific torque per phase RMS current of the SR machine, because the phase demagnetization is faster and negative torque production is thus avoided. Additionally, copper losses are reduced, since a lower current is required for the same torque, hence the machine efficiency should be higher. Additional calculations have shown that the use of soft-switching in the proposed converter causes a significant reduction of the thermal loading of the chopping devices, in comparison to a conventional hard-switching SRM converter. This

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APPENDIX I : MOTOR DATA

rated voltage	560 V
rated speed	1500 rpm
rated power	1100 W
stack length	80 mm
external stator diameter	120 mm
external rotor diameter	61.5 mm
air gap length	0.25 mm
stator yoke length	11 mm
rotor yoke diameter	20 mm
wire diameter	0.7 mm
iron	V800-500
stator pole angle	33°
rotor pole angle	33°

APPENDIX II : FLUX LINKAGE AND TORQUE DATA

Table II.1: Flux linkage in Vs versus phase current and rotor position.

i/A	0°	5°	10°	15°	20°	25°	30°	35°	40°	45°
0.0	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.5	0.37	0.34	0.28	0.24	0.18	0.13	0.08	0.04	0.03	0.03
1.0	0.71	0.65	0.56	0.47	0.37	0.27	0.15	0.08	0.07	0.06
1.5	0.93	0.88	0.77	0.64	0.51	0.36	0.21	0.10	0.09	0.08
2.0	1.03	1.00	0.89	0.75	0.59	0.43	0.26	0.14	0.12	0.11
2.5	1.10	1.06	0.97	0.82	0.65	0.48	0.30	0.18	0.15	0.14
3.0	1.14	1.11	1.02	0.87	0.70	0.53	0.35	0.22	0.18	0.17
3.5	1.18	1.15	1.06	0.91	0.74	0.56	0.39	0.25	0.21	0.20
4.0	1.21	1.18	1.09	0.94	0.77	0.60	0.43	0.29	0.24	0.23
4.5	1.24	1.21	1.12	0.98	0.81	0.64	0.46	0.32	0.27	0.26
5.0	1.26	1.23	1.14	1.01	0.84	0.67	0.50	0.36	0.30	0.29

Table II.2: Torque in Nm versus phase current and rotor position.

i/A	0°	5°	10°	15°	20°	25°	30°	35°	40°	45°
0.0	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.5	0.00	-0.13	-0.17	-0.19	-0.17	-0.18	-0.19	-0.04	-0.01	0.00
1.0	0.00	-0.46	-0.52	-0.60	-0.68	-0.62	-0.69	-0.17	-0.04	0.00
1.5	0.00	-0.97	-1.17	-1.26	-1.43	-1.40	-1.44	-0.38	-0.08	0.00
2.0	0.00	-1.46	-1.91	-2.09	-2.28	-2.45	-2.40	-0.67	-0.14	0.00
2.5	0.00	-1.88	-2.66	-3.06	-3.21	-3.45	-3.42	-1.04	-0.22	0.00
3.0	0.00	-2.25	-3.42	-3.96	-4.40	-4.55	-4.52	-1.49	-0.32	0.00
3.5	0.00	-2.57	-4.11	-4.87	-5.40	-5.52	-5.58	-1.93	-0.43	0.00
4.0	0.00	-2.88	-4.77	-5.80	-6.43	-6.65	-6.64	-2.46	-0.56	0.00
4.5	0.00	-3.17	-5.43	-6.75	-7.41	-7.60	-7.67	-3.14	-0.69	0.00
5.0	0.00	-3.46	-6.06	-7.75	-8.42	-8.68	-8.61	-3.90	-0.85	0.00

APPENDIX III : TRANSFER FUNCTIONS

Equation (5.21) - Transfer function for the variation of the clamp voltage in response to small changes in the clamp voltage reference: As indicated in section 5.1, the current that flows into the clamp capacitor can be averaged if the clamp capacitance is large, so that the clamp voltage changes much slower than the DC link oscillation. In this case, the variation of the average current in the clamp capacitor can be considered equal to the variation of the actuating signal I_c^{ref}, for small changes of the clamp voltage reference. The small-signal behavior of the clamp voltage control can be described by the block diagram shown in Fig. III.1.

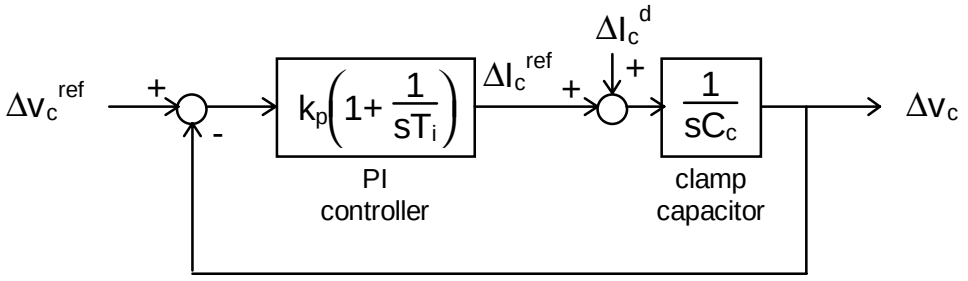

Fig. III.1: Small-signal block diagram for the clamp voltage control system.

If the disturbance input ΔI_c^d is neglected, the transfer function of the whole control system can be written as:

$$G(s)=\frac{\Delta V_c(s)}{\Delta V_c^{ref}(s)}=\frac{G_{PI}(s)\cdot G_{clamp}(s)}{1+G_{PI}(s)\cdot G_{clamp}(s)}=\frac{k_p\left(1+\frac{1}{sT_i}\right)\left(\frac{1}{sC_c}\right)}{1+k_p\left(1+\frac{1}{sT_i}\right)\left(\frac{1}{sC_c}\right)}.$$

If this transfer function is reduced to the standard form, then equation (5.21) is obtained:

$$G(s)=\frac{1+sT_i}{1+sT_i+s^2\frac{T_iC_c}{k_p}}.$$

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