Implementation of Two Topologies of a Low Cost Series Compensator for Voltage Sags

Abstract—In this paper two topologies of a low cost Series Compensator for Voltage Sags (SCVS) are introduced. Both topologies deliver to a sensitive load in a distribution system, three-phase sinusoidal balanced and regulated voltages, even under voltage sags. They differ, however, on where the diode rectifier is connected: at the in-bus or at the out-bus (regulated) of the SCVS. In order to validate the developed SCVS a prototype was implemented verifying the SCVS dynamics in the presence of a voltage dip caused by the turn-on of an inductive load, and harmonics due to the diode rectifier.

Keywords – voltage sag, custom power, power utility distribution system, short-circuit fault, power quality.

IV. INTRODUCTION

The concept of Custom Power has been familiar to industry experts since the beginning of the last decade, when the industrial and commercial customers of utilities have reported a rising tide of misadventures related to power quality. In this context the reliability concept have been changed in terms of short interruptions and voltage sags [6][7], among others aspects. Voltage sags are said harmful to critical loads and should be compensated in order to supply regulated voltage to such loads. The SCVS [1], represents a good choice to overcome such problems. By using this device it is possible to compensate voltage sags, harmonics and unbalances, in such way that the voltages delivered to the critical load are sinusoidal balanced and regulated. A SCVS is a system composed of a converter, a dc storage capacitor, and a transformer connected in series with a distribution bus-bar, which compensates for voltage disturbances on the bus-bar. The two topologies presented are improved versions of the SCVS proposed in [2], adding the harmonic and unbalance active compensations feature to the original project, as suggested by the authors. It is important to clarify that these particular implementations of a SCVS were done under certain costs restrictions. So, achieving a low cost configuration was a main concern of this project. The final goal is the implementation of a laboratorial prototype comparing the two proposed SCVSs, focused on a distribution system operation.

V. THE SCVS CIRCUIT AND ITS OPERATION

The block diagrams of the two topologies under investigation are presented in Fig. 1 (Topology I) and Fig. 2 (Topology II). Their principle of operation is based on the compensation of the positive-sequence voltage drop caused by the occurrence of voltage sags, as at the start up of huge induction motors, line short-circuits, etc [4]. Their improved control strategy also guarantees compensation for unbalances and harmonics, as will be presented.

The power circuit is composed by a three-phase diode full-bridge rectifier, a DC capacitor, a SPWM three-phase voltage-source inverter, a series transformer and a RLC low-pass filter.
The control strategy executed by the digital signal processor (DSP) in Fig. 1, measures the three-phase voltages of the in-bus \( v_{abc}^{in} \) and the out-bus \( v_{abc}^{out} \), and gives six digital-control signals that will command the three-phase inverter. The control scheme used in this SCVS is shown in Fig. 3 and most of its components are well discussed in [3].

The following definitions are used in the explanation of the control circuit:

- \( v_{in}^{a}, v_{in}^{b}, v_{in}^{c} \) – SCVS’s in-bus voltages.
- \( v_{a}^{in}, v_{b}^{in}, v_{c}^{in} \) – positive sequence components of voltages \( v_{abc}^{in} \), \( v_{abc}^{in} \), \( v_{abc}^{in} \).
- \( v_{out}^{a}, v_{out}^{b}, v_{out}^{c} \) – SCVS’s out-bus voltages (critical load).
- \( v_{har}^{a}, v_{har}^{b}, v_{har}^{c} \) – SCVS’s in-bus voltages without its positive sequence components. So, they are the harmonic and unbalanced components of the in-bus voltages.
- \( v_{d}, v_{b}, v_{c} \) – unit-value rms voltages synchronized with the in-bus positive sequence voltages components.
- \( v_{d}, v_{b}, v_{c} \) – control signals for voltage sag compensation.
- \( v_{d}, v_{b}, v_{c} \) – control signals for voltage sag, unbalance and harmonic compensation.
- \( v_{in}, v_{out} \) – voltages at the terminals of the SCVS’s series transformer, that were generated by the inverter.

Resuming the control operation, when the voltage-sags, harmonics or unbalances disturbances are detected, the control circuit calculates the compensation signals that the inverter uses as reference to produce the compensation control circuit calculates the compensation signals that the components.

According to equation (1), derived for phase A only. Its first term represents the fundamental positive sequence component, defining the voltage equation (2). The following terms define the voltage equation (3), and represent the unbalances (negative and zero sequences) and harmonics components.

In order to compensate the undesirable harmonics and/or unbalances, this algorithm uses a positive sequence detector, detailed in (3) and (2), to extract the voltages \( v_{a}^{in}, v_{b}^{in}, v_{c}^{in} \) from the measured voltages \( v_{abc}^{in} \), \( v_{abc}^{in} \), \( v_{abc}^{in} \) respectively. Therefore, the differences between them are the voltages \( v_{har}^{a}, v_{har}^{b}, v_{har}^{c} \), which represent the harmonics and unbalances components of the voltages in the in-bus. Thus, the control signals needed to compensate these disturbances must be the opposite of the voltages \( v_{har}^{a}, v_{har}^{b}, v_{har}^{c} \), and it is why they are subtracted from the voltage sags compensation signals.

\[
v_{in}^{a} = \sqrt{2} V_{a} \sin(o \omega_{f} \psi_{a}) + \sqrt{2} V_{b} \sin(o \omega_{f} \psi_{b}) + \sqrt{2} V_{c} \sin(o \omega_{f} \psi_{c})
\]

(1)

\[
v_{a}^{in} = \sqrt{2} V_{a} \sin(o \omega_{f} \phi_{a}) + \sqrt{2} V_{b} \sin(o \omega_{f} \phi_{b}) + \sqrt{2} V_{c} \sin(o \omega_{f} \phi_{c})
\]

(2)

\[
v_{har}^{a} = \sqrt{2} V_{a} \sin(o \alpha + \phi_{a}) + \sqrt{2} V_{b} \sin(o \alpha + \phi_{b}) + \sqrt{2} V_{c} \sin(o \alpha + \phi_{c})
\]

(3)

B. The voltage sag compensation algorithm

This algorithm ensures that the positive sequence components of the voltages \( v_{in}^{a}, v_{in}^{b}, v_{in}^{c} \), applied to the critical load, will be at their rated values.

First, the control voltages \( v_{d}, v_{b}, v_{c} \) are generated by the “Sin Generator” block. These control signals are pure sinusoidal waves, in phase with the in-bus fundamental positive-sequence voltage. To synthesize such signals, the use of a robust synchronizing algorithm is necessary. A phased-locked loop (PLL) algorithm tracks, continuously, the frequency of the in-bus fundamental positive-sequence voltage. The design of the PLL allows proper operation under high distorted and unbalanced system voltages. This PLL is also used by the positive sequence detector module of the previous algorithm, and is explained in [3] and [2].

The next step, and the goal of this algorithm, is to find the amplitude value for \( v_{d}, v_{b}, v_{c} \) to form the reference signal needed to compensate the voltage sag.

To understand how this amplitude signal is obtained, it is important to notice that the previous control block has already filtered the harmonics and unbalances present in the out-bus voltages, leaving only the fundamental positive-sequence component. So, the concept of the aggregate voltage calculation, defined by the equation (4), applied in these specific voltages, gives its representative three-phase line voltage rms value. An important feature of this definition is that it only needs the instantaneous value of those voltages.

\[
v_{\Sigma out}^{2} = v_{\Sigma out}^{2} + v_{\Sigma out}^{2} + v_{\Sigma out}^{2}
\]

(4)
By multiplying the aggregate voltage \(v_{\text{out}}\) by \(\frac{2}{\sqrt{3}}\), gives the amplitude of the out-bus phase-voltages \(v^a_{\text{out}}, v^b_{\text{out}}, v^c_{\text{out}}\). Then, this amplitude signal is compared with the reference of 1 pu giving an error signal which is used as the input of the PI controller, which acts as a supervisory signal in order to assure a zero steady-state error. Another error signal, calculated by the comparison between the reference value and the actual value in the terminals of the series transformer, caused by the power low-pass RLC filter in the output of the inverter.

C. SPWM voltage control algorithm

The conventional Sine PWM (SPWM) techniques are based on the comparison between the control signal and a triangular waveform. The frequency of the triangular waveform establishes the inverter switching frequency and generally is kept constant along with its amplitude [5].

In this work, the algorithm used to control the inverter is based on an improved Sine PWM voltage control technique proposed in [3], which intends to minimize the deviation between the reference value and the actual value in the terminals of the series transformer, caused by the power low-pass RLC filter in the output of the inverter.

VI. EXPERIMENTAL RESULTS

The closed loop performance of the equipment was verified with a 50kVA prototype operating on a 220Vrms (line-to-line) testing system. Load A is a critical load that must be protected against voltage sags. An inductive Load B can be connected to the in-bus through the switch SW1, inducing a voltage dip at this bus.

The tests performed with the set-up described above confirm the main purpose of the SCVS and account for the harmonic compensation.

The results presented below were obtained with the two topologies shown in Figs. 1 and 2.

A. Load B disconnected

Figs. 4 and 5 for Topologies I and II respectively, show the operation of the equipment compensating a natural sag of approximately 23V, caused by Load A. One can see also the current flowing through the secondary of the transformer.

B. The Load B connection

Fig. 6 shows the Load B connection transient, for Topologies I and II respectively, and the immediate rising of the compensation voltage. It is also shown that the connection of the Load B emphasizes the voltage sag effect at the in-bus, while the out-bus voltage is kept regulated. As one can see the in-bus voltage is distorted due to the harmonics presented in the line current generated by the rectifier. The current flowing through the transformer is clearly more distorted for the Topology II because, in this case, the rectifier current is approximately 23V, caused by Load B.
Fig. 4: Topology I, Load B disconnected. Orange, in-bus $V_{AB}$ (100V/div); Blue, regulated $V_{AB}$ (100V/div); Purple, compensation voltage $V_C$ (50V/div); Green, current through phase C (10A/div); Time (10ms).

Fig. 5: Topology II, Load B disconnected. Orange, in-bus $V_{AB}$ (100V/div); Blue, regulated $V_{AB}$ (100V/div); Purple, compensation voltage $V_C$ (50V/div); Green, current through phase C (10A/div); Time (10ms).

Fig. 6: Load B connection transient. a) Topology I; b) Topology II: Orange, in-bus $V_{AB}$ (100V/div); Blue, regulated $V_{AB}$ (100V/div); Purple, compensation voltage $V_C$ (50V/div); Time (10ms).

C. The voltage sag and harmonics compensation

Due to the three-phase full-bridge diode rectifier, the current at the input of the SCVS carries some significant low order harmonics that distorts the in-bus and the out-bus voltages.

With the Load B connected Figs. 7 and 8 show the results, for Topologies I and II respectively, when both the voltage sag compensation algorithm and the harmonics compensation algorithm are present. One can observe the typical flattening at the wave tops caused by the odd harmonics generated by the rectifier. Note that in both cases the out-bus voltage is regulated at the rated rms value without the flattening.

We must unfortunately point out, however, the presence of some harmonics in the regulated voltage. Some extra work must be done in order to improve the passive filter and overcome this problem.

D. The regulated dc bus voltage

Fig. 9 shows the dc voltage for the Topology II. One can see that its value is not affected by the voltage sag and is kept regulated at its rated value.
Fig. 7: Topology I, Load B connected. Orange, in-bus $V_{ab}$ (100V/div); Blue, regulated $V_{ab}$ (100V/div); Purple, compensation voltage $V_c$ (50V/div); Green, current through phase C (10A/div); Time (10ms).

Fig. 8: Topology II, Load B connected. Orange, in-bus $V_{ab}$ (100V/div); Blue, regulated $V_{ab}$ (100V/div); Purple, compensation voltage $V_c$ (50V/div); Green, current through phase C (10A/div); Time (10ms).

Fig. 10: Topology II. Orange, in-bus $V_{ab}$ (300V/div); Blue, regulated $V_{ab}$ (300V/div); Purple, dc link voltage $V_d$ (300V/div); Green, current through phase C (5A/div); Time (10ms).

and harmonics. Both Topologies
This is just a preliminary work and with the obtained results one cannot yet conclude on which Topology is the better one. Further work will be carried out in order to identify more details and clarify the behavior of these two topologies.

REFERENCES

VII. CONCLUSIONS
A laboratorial prototype of a SCVS was implemented which allows to verify the operation of two topologies. A complete set of experimental results of both topologies was presented, with emphasis on the compensation of voltage sags.