A practical implementation scheme for Component Simulation SI filters

Jones Schechtman, Antônio C. M. de Queiroz, and Luiz P. Calôba
Programa de Engenharia Elétrica - COPPE & EE, Universidade Federal do Rio de Janeiro
CP 68504, 21945-970 Rio de Janeiro, RJ, Brazil

Abstract **—This paper presents a very practical method to implement the new switched-current structures recently proposed by the authors. Those structures are obtained by a one-to-one simulation of the components of a continuous-time Transconductance-C model. The resulting circuits operate with doubled sampling rate (sampling the input and updating the output at each phase), don't present switching glitches, use the minimum possible number of switches and naturally admit two-phases nonoverlapping clocks. Two versions are presented, with "direct" or "modulated" signals. The "modulated" version presents low sensitivity and first-order cancellation of clock feedthrough effects.**

I. Introduction

Switched-current (SI) filter designs are usually based on state-variable methods using integrators or wave techniques [2][3][5][6]. A different approach based on a direct SI simulation of continuous-time capacitors and transconductors was presented in [1], that easily implements bilinear or Euler mappings, with doubled effective sampling rate and glitchless operation (due to the absence of current-conducting switches, as used in "second-generation" structures [4]). In this paper, the basic synthesis procedure for the bilinear mapping is reviewed, and an economical general implementation scheme is presented for the synthesis of these SI filters. Two versions are described: with "direct" or "modulated" signals. The "modulated" version is better, due to its inherent low sensitivity and first order cancellation of the clock feedthrough effects.

II. SI transconductances and transcapacitances

Transconductance-C continuous-time structures can be directly mapped into bilinear SI circuits, by the use of the correspondence of continuous-time transconductances and transcapacitances to switched-current versions presented in fig. 1. This mapping is obtained by comparing the continuous-time nodal equation (1) and the same equation (2) after the application of the bilinear time-discretization formula. The same procedure can be used for Euler formulas [1]. Note that the circuit is symmetric from phase to phase and T is the period of one switching phase (this is the effective switching period and z^{-1} is the delay of one phase). This effectively doubles the sampling rate.

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$$s\mathbf{C}\mathbf{v}(s)+\mathbf{G}\mathbf{v}(s)+\mathbf{i}(s)=\mathbf{0} \quad (1)$$

$$\left(1-z^{-1}\right)\frac{\mathbf{C}}{T}\tilde{\mathbf{v}}(z)+\left(1+z^{-1}\right)\frac{\mathbf{G}}{2}\tilde{\mathbf{v}}(z)+\left(1+z^{-1}\right)\frac{1}{2}\tilde{\mathbf{i}}(z)=\mathbf{0} \quad (2)$$

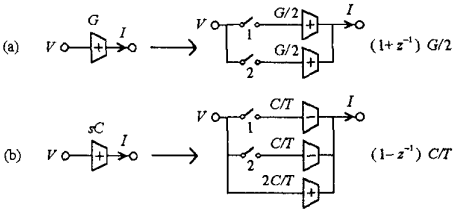

Fig. 1. Bilinear "SI transconductance" (a) and "SI transcapacitance" (b).

Combining these basic blocks it is possible to synthesize the SI filter directly from the continuous transconductance-C prototype. The first step is to transform the capacitors in transcapacitances (fig. 2). The second step is to substitute the transconductances and transcapacitances by its SI versions (Fig. 1). A simple example is the Transconductance-C integrator shown in fig. 3. In general the circuit can be simplified by the elimination of redundant switches and reduction of the number of the inverting stages.

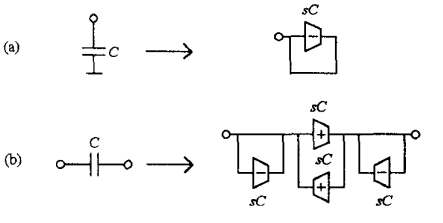

Fig. 2. Grounded capacitor and floating capacitor construction using transcapacitances.

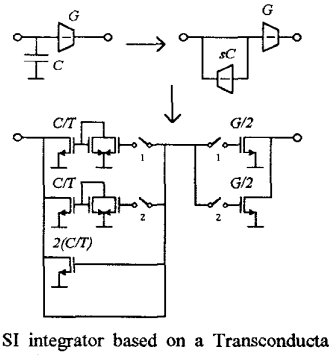

Fig. 3. A bilinear SI integrator based on a Transconductance-C continuous prototype. The input and output are in current. The implementation done is the most trivial and without any simplification.

III. A GENERAL IMPLEMENTATION SCHEME

The SI circuit obtained by this technique is node-by-node equivalent to the prototype. A very practical and systematic implementation with a reduced number of components can be obtained by noting that :

1) The nodal voltages are sampled at phase 1, phase 2 or both (this means that only two switches for each node are necessary).

2) The currents injected in each node are direct or inverted currents (each node must have a direct and a inverting input for currents).

These two observations are realized by the circuit of fig. 4, that represents a "general" node. As an example the integrator of fig. 3 is re-implemented using this scheme (fig. 5)

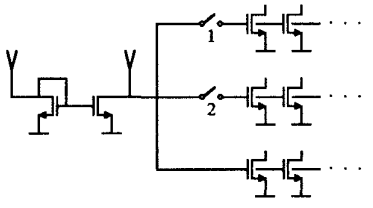

Fig. 4. A "general node" of the SI circuit.

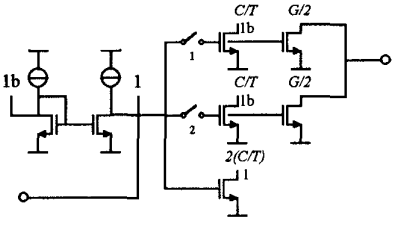

Fig. 5. Re-implementation of the integrator of fig.4 using the proposed scheme.

A continuous time transconductance-C circuit of a low-pass 5th order elliptic filter is presented in fig. 6. The circuit is a direct simulation of an LC doubly terminated ladder structure. The switched-current version (bilinear) of this circuit is shown in fig. 7. The input and output are sampled and updated at the two phases, doubling the effective sampling rate. The total number of switches is the minimum possible (two times the number of nodes of the original model) and the circuit doesn't use current conducting switches. Note that the number of inverters is equal to the number of nodes of the model. These inverters can be completely removed in a balanced structure but at the cost of duplicating the circuit. The frequency response of the circuit is shown in fig. 8. The simulation was made with the ASIZ program [2], with error margins computed by sensitivity analysis, assuming 2% random errors in all the transistor transconductances. The circuit was designed for 10:1 ratio between the switching frequency and the passband border frequency. In the normalized simulation, to obtain a pass-band border frequency at 0.2 Hz, it was used a switching frequency of 1 Hz only (one half of the effective sampling rate).

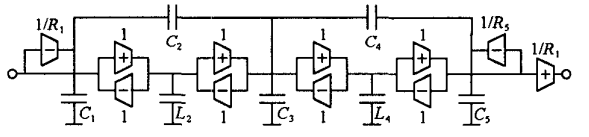

Fig. 6. Schematic representation of the continuous time transconductance-C 5th-order elliptic low-pass filter.

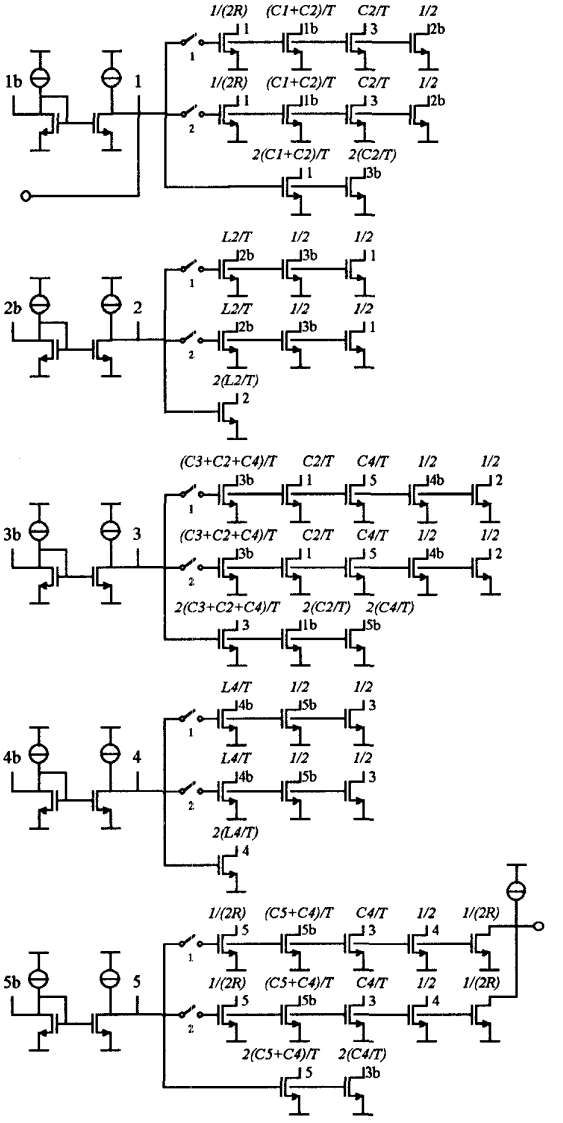

Fig. 7. The SI bilinear low-pass 5th order elliptic filter. The circuit operates sampling the input and updating the output at each phase effectively doubling the switching frequency. Note that the circuit doesn't use current conducting switches.

As can be seen in fig. 8, the circuit is relatively sensitive to component variations. The "three-way" structure that implements the SI transcapacitance is very sensitive. A mismatch between the continuous and switched parts introduces a parasitic $(1+z^{-1})C/T$ term that is not present in the original model. The situation becomes worst as T becomes small. This problem is solved by the version that uses modulated signals.

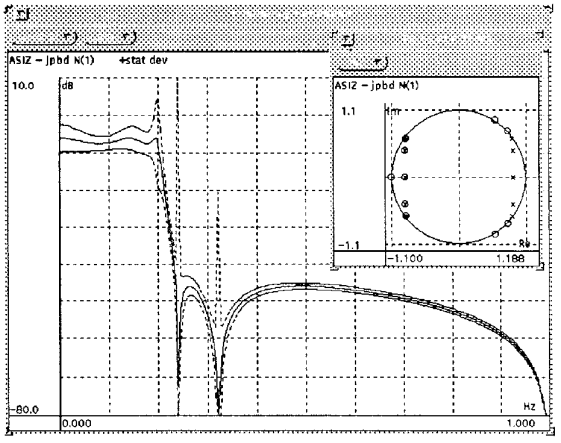

Fig. 8. Gain frequency response of the "non-modulated" bilinear SI low-pass filter, with expected error margins and poles and zeros. It is relatively sensitive to component variations.

IV. THE SIGNAL MODULATED VERSION

A modulator is a circuit that changes the sign of the signal at each phase. The modulation and demodulation process (fig. 9) transform $(1+z^{-1})$ in $(1-z^{-1})$ and the reverse too. This permits to exchange the implementation of the SI transconductance and the SI transcapacitance (fig. 10).

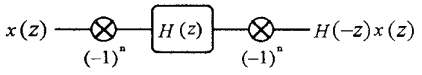

Fig. 9. Modulation and demodulation process.

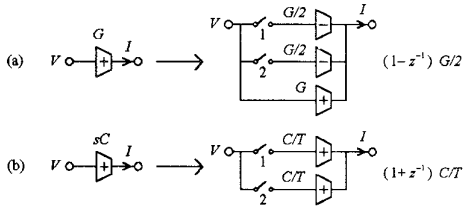

Fig. 10. Bilinear "SI transconductance" and "SI transcapacitance". Admitting that the whole circuit has "modulators" at the input and output.

The modulators don't affect the sensitivity of the circuit. In this new situation, the "three-way" components become comparatively small as T becomes small. This means that the sensitivity becomes better with small T.

The implementation of the input modulator is shown in fig. 11. The same modulator circuit can be used at the output but a simplification can be done by incorporating the modulator with the "SI transconductance" that appears at the output stage of the filter. This simplification is shown in fig. 12. The complete SI-filter using modulated signals is presented in fig. 13. It implements the Transconductance-C model by using the SI transconductances and transcapacitances of fig. 10. The output modulator is incorporated in the output stage. As previous discussed the circuit has low sensitivity (as can be observed in the frequency response presented in fig. 14). It also does a first order cancellation of the clock feedthrough because the signals in all the nodes are inverted at each phase canceling the charge injected at the previous phase. Note that the number of switches is only two above the absolute minimum.

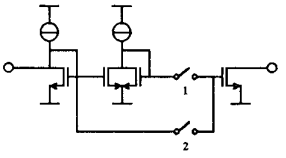

Fig. 11. Modulator circuit. Note that is doesn't use current conducting switches. The input and output are in current.

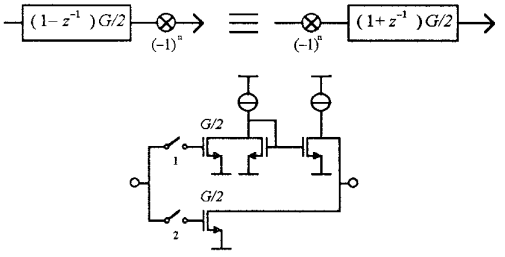

Fig. 12. The output modulator can be incorporated in the "switched transconductor" at output stage of the filter.

V. CONCLUSION

A practical and systematic implementation scheme for the switched current structures previously proposed by the authors was presented. The resulting circuits operate with doubled effective sampling rate, what allows for two times faster filters, as also happens with the method in [5]. However, they don't present switching glitches, because of the absence of current conducting switches usually employed in second generation structures. In the modulated version they have low sensitivity to component variations and do a first order cancellation of the clock feedtrough. The circuits presented also use the minimum number of switches and the minimum number of inverters for a non-balanced circuit. A balanced implementation can be built but with the cost of nearly doubling the circuit size, without much advantage, since the modulated version also does a first order cancellation of the clock feedtrough. The fact that the

synthesis procedure is directly derived from the synthesis of a transconductor-C prototype allows the direct use of known structures as biquads and the various forms of passive filter simulations developed for that technology.

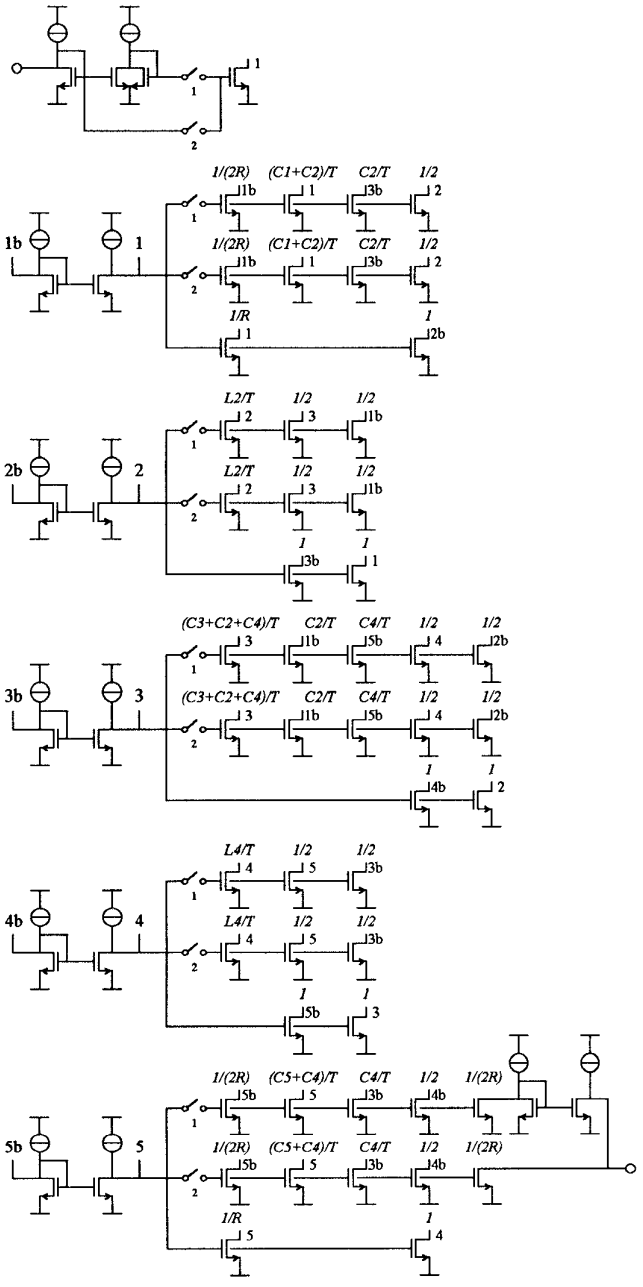

Fig. 13. The SI bilinear 5th order elliptic low pass filter, using modulated signals. It has low sensitivity to component variations and does a first order cancellation of the clock feedtrough. The input and output are in current. The input modulator is at the top of the figure and the output modulator is incorporated at the last stage of the filter.

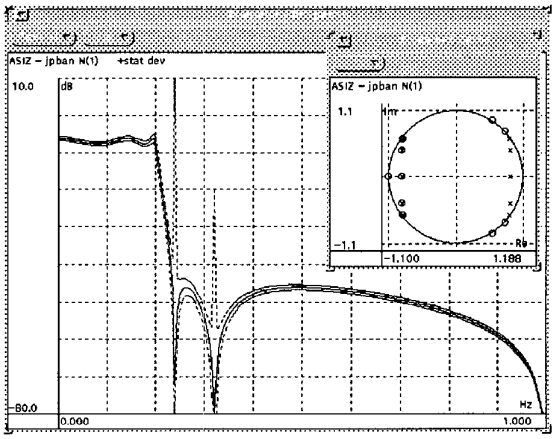

Fig. 14. Gain response of the "modulated" SI bilinear low pass filter of fig. 11. Note the low sensitivity to component variations.

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