A High Performance Balanced MOS Transconductor

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***Abstract* — An easily tunable high frequency balanced transconductor without internal nodes and with a low output conductance is presented. The structure uses only 7 MOS transistors. The output conductance can be independently adjusted (in order to be canceled) without affecting the transconductance. The transconductor also guarantees the common-mode stability of balanced filter structures. The simulation results of a 5th order elliptic low-pass filter, using standard CMOS 2 µm process, at 100 MHz with *Q* and frequency controls are shown.**

I. Introduction

The major limitation in the frequency response of transconductance-C filters are the parasitic poles of the circuit. Some parasitic poles are associated with signal inversion (or current mirrors) and can be eliminated by a balanced design [1]. Other parasitic poles arise when cascode techniques are employed in order to obtain a low conductance at the output of the transconductors [2, 3]. Very high frequency filters can be constructed if the transconductor doesn't present any internal nodes. This can be obtained by the adoption of a balanced design and a technique that compensates the output differential conductance without the introduction of any additional nodes [4].

This paper discusses the synthesis of transconductance-C balanced structures, the common-mode stabilization of them, and presents a balanced transconductor without internal nodes, that has as advantages over previous proposed structures, the use of a fixed low supply voltage and the completely independent control of the output conductance. The output conductance (G_{out}) can be adjusted from negative to positive values without disturbing the bias voltage nor the transconductance (G_m). Very high G_m/G_{out} ratios can be possible as long as the components can be matched.

II. Transconductance-C balanced structures

The usual synthesis process for precision transconductance-C filters is the simulation of the inductors by capacitors and gyrators. Lets take as an example the 5th order passive filter of figure 1. The active transconductance-C version of this circuit is shown in figure 2. The positive transconductances are usually implemented as two inverting stages (or with a current mirror), introducing a parasitic pole in the structure. The positive transconductors can be eliminated by a balanced structure.

The balanced version can be implemented by duplicating the single-ended version and substituting the positive transconductors by negative ones with symmetric input voltages [1] (fig. 3). This means that we can implement balanced filters, without any parasitic poles created by the transconductors, as long as the negative transconductors doesn't have any internal nodes.

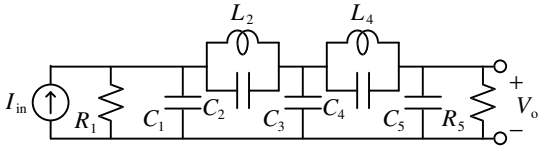

Fig. 1. 5th-order elliptic low-pass filter.

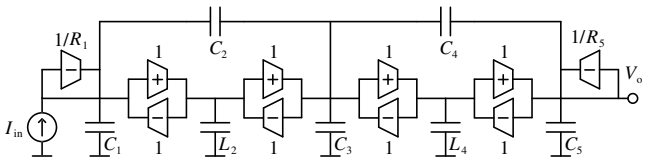

Fig. 2. Active transconductance-C version of the filter in fig. 1

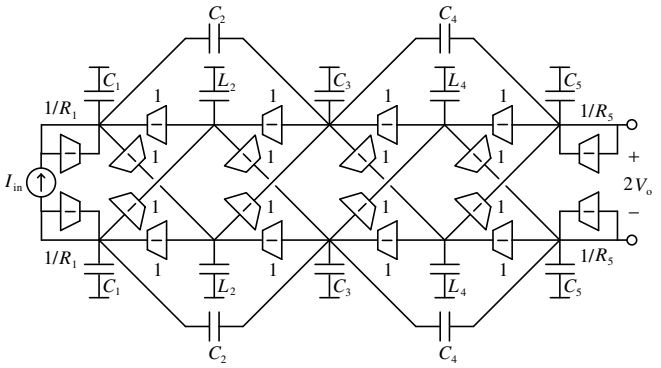

Fig. 3. Balanced version of the circuit in fig. 2.

The balanced circuit has, however, the double of the number of poles of the original passive version. Half of them corresponds to the original passive structure but the other half doesn' t.

To understand the origin of the other poles it is necessary to do a transformation of variables. The original system of equations describing the circuit with nodal voltages (V_1, V_1' V_2 ,V_2' , ...,V_n ,V_n') is transformed by the following linear transformation, applied to each pair of symmetric nodes k and k' :

$$\begin{aligned} Vc_k &= \left(V_k + V_k'\right)/2 \qquad k = 1..n \\ Vd_k &= \left(V_k - V_k'\right)/2 \end{aligned} \tag{1}$$

Each pair of nodal voltages is transformed into two other variables: the common-mode voltage (Vc_k) and the differential-mode voltage (Vd_k). The nodal equations of a perfectly symmetric balanced circuit can be decomposed, after the above transformation, into two independents systems of equations corresponding to these

two sets of transformed variables. These two systems of equations can be interpreted as two independent circuits: the differential-mode circuit and the common-mode circuit.

The poles corresponding to the original passive structure are those of the differential-mode circuit and the other poles are those of the common-mode circuit.

The differential-mode circuit is identical to the single-ended structure (fig. 2). The common-mode equivalent circuit can be easily obtained by assuming that the differential voltages are null. This can be done by short-circuiting the symmetric nodes of the balanced version and dividing by 2 all the remaining conductances, capacitances, and current sources. The resulting circuit is draw in fig. 4.

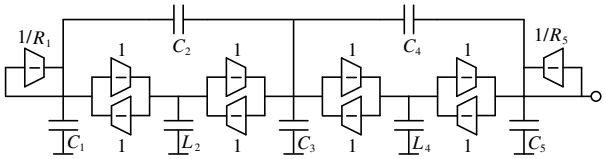

Fig. 4. Common-mode circuit corresponding to the filter in fig. 3. Note that all the transconductances are negative.

The closed positive loops indicate a potential instability (the behavior is very like the one of a "flip-flop"). An analysis of this circuit demonstrates the existence of poles in the right-side of the *s*-plane. If the filter is implemented with floating capacitors (replacing the pairs of grounded capacitors in fig. 3), the corresponding common-mode circuit has the same structure of fig. 4, but with the grounded capacitors being parasitic capacitors. The result is just a faster "flip-flop".

Since the common-mode circuit and the differential-mode circuit are independent, the poles of one are non-observable by the other. This means that the differential response of the balanced filter is not perturbed by the common-mode poles (they are covered by zeros). The poles and zeros of the differential response of the balanced-filter is shown figure 5.

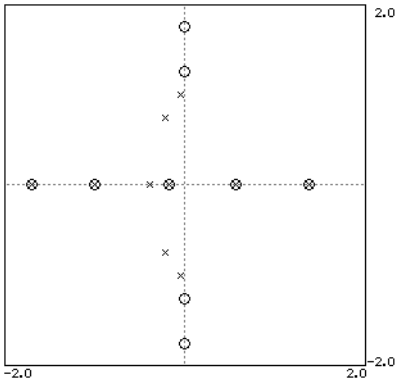

Fig. 5. Poles and zeros of the differential frequency response of the balanced filter of fig. 3. The circuit is unstable

As can be seen it has non-observable poles corresponding to the common-mode circuit. Part of them are at the right-side of the *s*-plane causing instability. Despite the fact that they are non-observable in the differential response, the filter will not work. The common-mode circuit must be stabilized.

III. Common-mode stabilization

Common-mode circuit stabilization can be obtained if high conductances to ground are added to all the nodes of the common-mode circuit. This moves the common-mode poles to the left stabilizing the common-mode circuit. But such conductances cannot appear in the differential-mode circuit, or the desired transference is affected. So, we need a device that acts as a grounded conductance in the common-mode circuit but as an open circuit (low conductance) in the differential-mode circuit. The device of figure 6, here called a "stabilizer", has this property.

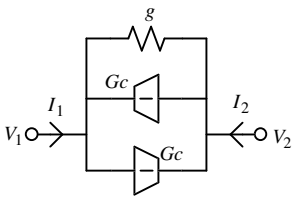

Fig. 6. "Stabilizer" circuit.

The terminals are connected to symmetric nodes of the balanced filter. The nodal equations of the stabilizer are the following :

$$\begin{aligned} I_1 - (V_1 - V_2)g - GcV_2 = 0 \\ I_2 + (V_1 - V_2)g - GcV_1 = 0 \end{aligned} \tag{2}$$

that after the transformation (1), results in:

$$\begin{aligned} Ic = GcVc \\ Id = (2g - Gc)Vd \end{aligned} \tag{3}$$

This means that in the common-mode circuit the stabilizer corresponds to a grounded conductance of value *Gc* and the conductance *g* has no effect. The common-mode stability is strictly guaranteed by the crossed transconductors. In the differential-mode circuit the stabilizer corresponds to a grounded conductance of value $2g–Gc$. The crossed transconductors produce the negative conductance.

If the conductance *g* is adjusted to be equal *Gc*/2, the total conductance introduced in the differential-mode circuit is zero. By controlling the value of *g*, it is possible to introduce negative or positive conductances to ground at the nodes of the differential-mode circuit without any perturbation in the common-mode circuit. This can be useful for the compensation of the output conductances of real devices and for global *Q*-tuning.

The minimum conductance value (*Gc*) that needs to be added to a node of the common-mode circuit in order to guarantee the stability, equals the absolute sum of all the transconductances (of the common-mode circuit) with output at that node. This guarantees a voltage attenuation at DC and is enough to move all the common-mode poles to the left of the *s*-plane. This can be easily accomplished in the balanced structure by adding an "stabilizer" at each pair of symmetric transconductors outputs, with the *Gc* value "strictly" greater then its transconductances G_m. In some cases, where the common-mode circuit has already grounded conductances (as in fig. 4) this condition can be relaxed.

The poles and zeros of the differential response of the balanced filter with an "stabilizer" at the output of each pair of symmetric transconductors (with $Gc = G_m$ and $g = Gc/2$) is plotted in figure 7. All the common-mode poles (covered by zeros) were moved to the left-side of the *s*-plane. The differential-mode poles

can be moved to the left or right by adjusting the value of g. This corresponds to a global Q-control of the filter. Since g doesn't appear in the common-mode circuit, this control doesn't disturb the common-mode poles.

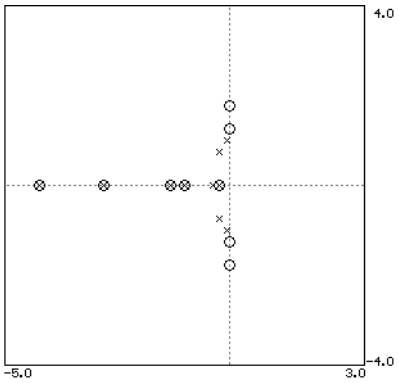

Fig. 7. Poles and zeros of the frequency response of the balanced filter, with the "stabilizers". The circuit is now stable.

IV. The Transconductor

Figure 8 presents the proposed balanced transconductor, embedded with a "stabilizer" circuit at the output, built with MOS transistors. The transconductance (G_m) is defined by the symmetric transistors M_1, M_2 and is adjusted by the current sources M_6, M_7. The crossed transistors M_3, M_4 implements the transconductances Gc of the stabilizer structure and, must be equal or wider then M_1, M_2. They guarantee the common-mode stability but, as discussed, introduce a differential negative conductance that is compensated by the conductance g of the stabilizer, implemented by the transistor M_5 operating in the linear region. This conductance can be adjusted by controlling the gate voltage V_Q of the transistor. A complete cancellation of the negative conductance introduced by the crossed transistors is obtained when g equals $Gc/2$.

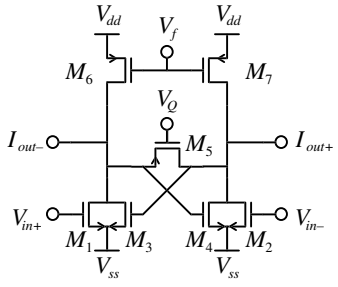

Fig. 8. Balanced transconductor embedded with the "stabilizer" circuit, built with MOS transistors.

By reducing g, controlling V_Q, the output conductance of all the transistors can also be completely canceled as long as the components can be matched. The output conductance can be varied from negative to positive values without disturbing the circuit bias or transconductance. Note that a change in the transconductance (by V_f) affects the output conductance, that must be readjusted. Because of the balanced structure, linearity is improved by cancellation of the even-order non-linear terms.

The transconductor was simulated using SPICE with the structure shown in figure 9. The first transconductor (T_1) is used to correctly generate the common-mode bias voltage at the input of T_2, permitting the use of a floating input voltage source. The input of a practical filter may be exactly in the same way, with the signal coupled by a transformer without a center tap. The supply voltage used was of 5 V, and the process is a CMOS 2μm one.

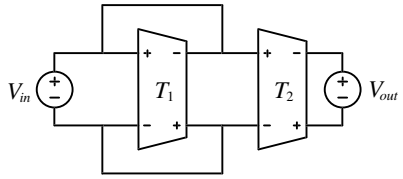

Fig. 9. Test structure for the transconductor. T_1 allows the use of a floating input voltage, and V_{out} is used for current and output conductance measurements.

Figure 10 depicts the transconductance as a function of the input voltage (with V_{out}=0). The distortion is basically of 3rd order, and is below 0.5 % for a 1 V peak-to-peak input. The output conductance relation $V_{out} \times I_{out}$ with V_{in} = 0 for different values of V_Q is shown in figure 11. It can be observed that the output conductance (curve slope) can be varied from positive to negative values with high g_m/g_{out} ratios attainable.

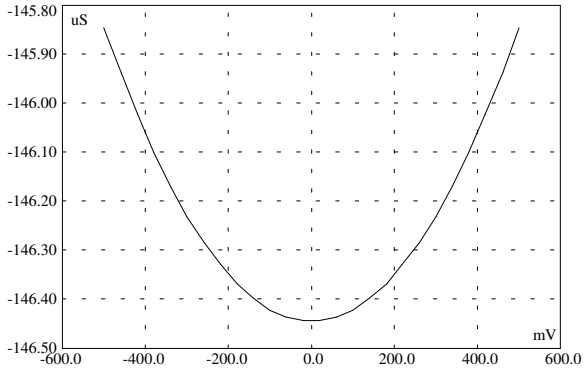

Fig. 10. Transconductance as a function of the input voltage, when V_{out}=0.

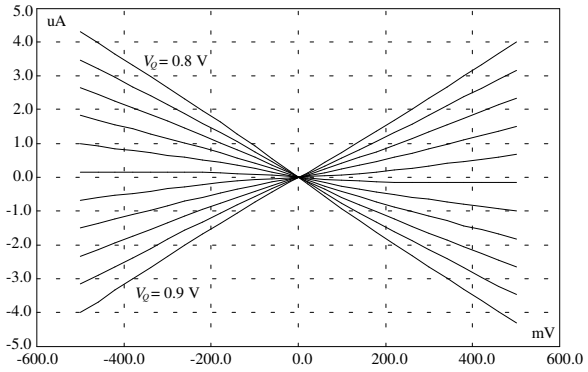

Fig. 11. $I_{out} \times V_{out}$ characteristic for various values of V_Q, showing the tuning of the output conductance.

As there are no parasitic poles, except the ones dictated by the distributed nature of the transistors, the maximum natural frequency for a filter using this transconductor is limited solely by the ratio of the transconductance to the input capacitance and other parasitic capacitances. The above transconductor connected as a resistor (closed loop), was simulated with SPICE and presented a natural frequency of approximately 850 MHz.

V. A FILTER SIMULATION WITH SPICE

As an example, the balanced 5th-order elliptic filter of fig. 3, with the symmetric pairs of transconductors substituted by the proposed balanced transconductors (fig. 8), was simulated with SPICE. The cutoff frequency was designed to be of 140 MHz, The frequency response obtained is plotted in the figure 12. The frequency distortion of the response is caused by the gate capacitances (about 1/6th of the main capacitances), this can be corrected by discounting these values from the values of the filter capacitances. Filters can be built using only gate capacitances in order to obtain a better matching of components. The curve also shows the effect of the adjustment of V_Q. By lowering V_Q the output conductance of the transconductors becomes higher and the result is a reduction of the filter poles' Qs. A higher value of V_Q introduces a slightly negative conductance at the outputs and results in an enhancement of the Qs. The curves shown correspond to a variation from 0.84 V to 0.86 V in the voltage V_Q.

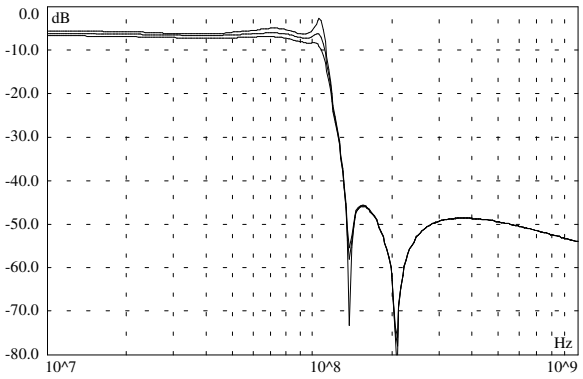

Fig. 12. Frequency response simulation of the test filter, showing the effect of Q-tuning.

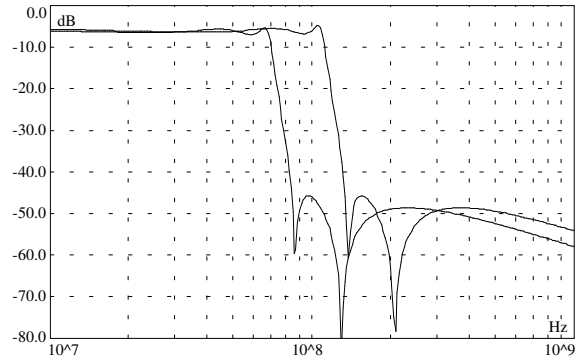

Fig. 13. Frequency response simulation of the test filter, showing the effect of frequency tuning.

Figure 13 shows the effect of varying V_f (and readjusting V_Q in order to obtain the correct Qs). The passband edge frequency could be varied from 70 to 110 MHz without a significant reduction of the linearity (V_f changes the circuit bias voltage and a reduction of the bias voltage degrades the linearity of the transconductors). The total harmonic distortion of the filter was estimated as below 1 % for an input voltage of 0.5 V peak-to-peak.

VI. CONCLUSION

A versatile balanced transconductor, suitable for the construction of very high frequency transconductance-C filters was presented. It has as advantages over previously proposed structures the easy and independent tuning of the output conductance and transconductance, and the use of a fixed low supply voltage. The circuit also guarantees the common-mode stability of balanced structures. Because the bias and the transconductance are not affected by the control of the output conductance, the proposed transconductor is specially useful in the synthesis of directly coupled cascade realizations, where there is a need of an independent control of the Q of the sections.

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