Switched-Current Ladder Band-Pass Filters

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ABSTRACT

This work discusses the implementation of band-pass filters derived from passive ladder prototypes using switched-current techniques. The bilinear transformation is applied to a set of modified state equations derived from a conveniently modified passive prototype filter, and from the equations a switched-current circuit is derived. Two different approaches are studied and compared by simulation.

I. INTRODUCTION

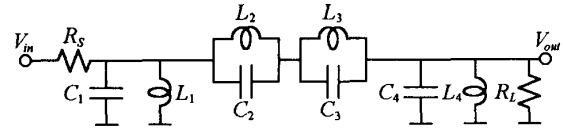
The design of switched-current (SI) filters using the bilinear transformation has been receiving some attention recently. The application of the bilinear s-to-z transformation to continuous-time prototype filters is considered the most adequate method for the generation of highly selective low sensitivity discrete-time filters, due to the preservation of gain characteristics and sensitivities, and the low sensitivities that result if the prototype filter is an LC doubly terminated structure with maximum power transfer.

In [1], a method previously used for the generation of switched-capacitor (SC) low-pass filters [2] was adapted for switched-current realization. It resulted in a very simple structure, using essentially only backward and forward Euler SI integrators directly connected without the help of inverters. In [3], [4], and [5], low-pass filters with true bilinear integrators were demonstrated. Those filters result in substantially more complex structures, due to the bilinear integrators, but can present better sensitivity characteristics due to the more perfect simulation of the original prototypes.

In this paper, the realization of band-pass filters using the bilinear transformation applied to passive prototype filters is discussed. In section II, the choice of a convenient passive prototype is studied, with considerations about necessary transformations to allow a stable state-space simulation. In section III, the same procedure used in [1] for the realization of low-pass filters is extended to the band-pass case, with some observations on how to apply it to the general filter case. In section IV a realization using true bilinear integrators is derived, and in section V the two realizations are compared. To the knowledge of the authors, no previous work was published about SI band-pass filters with finite transmission zeros using a state-variable approach. (In [5] there is an example of a polynomial filter design using wave filter techniques.)

II. PASSIVE PROTOTYPES FOR BAND-PASS FILTERS

As example, a 6th-order elliptic band-pass filter with geometrically symmetrical gain characteristics will be used. The prototype is obtained by well-known methods, and includes the usual pre-distortion for the application of the bilinear transformation. Fig. 1 depicts the normalized prototype, that in the discrete-time version results in a passband with 1 dB maximum attenuation, from 0.8 to 1.2 Hz, for a sampling frequency of 5 Hz, and a stopband minimum attenuation of 40 dB.



R_S=R_L=1; C_1=3.081674; L_1=0.248147; L_2=0.654218; C_2=0.293501; L_3=2.605475; C_3=1.168890; C_4=3.081674; L_4=0.248147

Fig. 1. Normalized LC doubly terminated prototype. Units in Ω, F, and H.

The writing of state equations for this structure presents two problems: The first is the capacitor loop. One of the capacitors cannot have its voltage as state variable because it is dependent from the three other capacitor voltages. The problem is solved as usual, with the replacement of one of the capacitors by a voltage-controlled current source. In this case, to avoid breaking the symmetry of the structure, both C_2 and C_3 are transformed, and the central nodal voltage (V_2) is used as state variable. The state equations for the capacitor voltage variables now include a direct coupling among states (and so are not properly "state equations"). The other problem is the inductor loop. The inductor currents cannot be simulated without transformation, because they can include an indeterminate DC component (the structure presents a natural frequency at s=0). The solution is to use Thévenin equivalents to eliminate the loop and the extra natural frequency. The transformed prototype is shown in fig. 2. Certainly it is not perfectly equivalent to the original circuit in terms of sensitivity, but the degradation is not high.

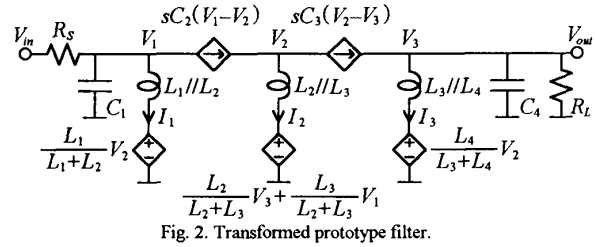


Fig. 2. Transformed prototype filter.

This prototype is equivalent to the one used in [6], where the synthesis of switched-capacitor band-pass filters is studied. The circuit transformations shown in the next section are also similar to

the ones developed there, but a different point of view is used.

III. BILINEAR SI SYNTHESIS OF BAND-PASS FILTERS USING BACKWARD AND FORWARD EULER INTEGRATORS

The transformations used in [1] on the prototype passive filter, in order to allow the writing of a z-domain state-space system of equations containing only backward Euler and forward Euler integrations (except for one bilinear integration: of the input signal), can be summarized as (see fig. 3):

- Capacitors are not modified. Their voltages (or linear combinations of some of them, as in the system that results from the circuit in fig. 2) are used as state variables directly. These voltages will be generated by backward Euler integrations of current variables and weighted sums with other voltages.
- Inductors L_x are transformed into parallel LC tanks with negative capacitors, where the added capacitances are $C_x=T^2/(4L_x)$, where T is the sampling period. These added capacitances must be compensated with another, positive, capacitances in parallel with the LC tanks. The currents in these LC tanks will be state variables, generated by forward Euler integrations of voltage variables, and will be simulated multiplied by $(1+z^{-1})/2$.
- Resistors R_y are transformed into parallel positive RC circuits, where $C_y=T/(2R_y)$. The added capacitances must be compensated with another, negative, capacitances in parallel with the RC circuits. This transformation has the effect of transforming the integration of V/R_y terms that appear in the equations generating voltage variables (on the capacitors adjacent to the terminations, in the case) into backward Euler integrations.

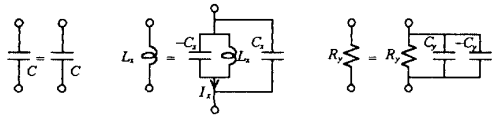


Fig. 3. Transformations in circuit elements to allow z-domain state equations with Euler integrations.

These relations can be verified by writing the state equations for the circuit in the s-domain and transforming them into the z-domain by the bilinear transformation:

$$s \to \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{1}$$

By applying these transformations to the prototype in fig. 2, the circuit in fig. 4 is obtained. Note that the capacitors added to compensate the negative capacitors in the LC tanks were also transformed into voltage-controlled current sources, because their voltages are dependent on the voltage variables used.

The writing of s-domain modified state equations for this circuit, and the subsequent application of the bilinear transformation (1) results in:

$$V_1 = \frac{T}{C_1 - C_S + C_2 + C_a}\frac{1}{1-z^{-1}}\left(\frac{V_{in}}{R_S}\frac{1+z^{-1}}{2} - \frac{V_1}{R_S} - I_1\frac{1+z^{-1}}{2}\right) + \frac{C_2 + \frac{C_a L_a}{L_2}}{C_1 - C_S + C_2 + C_a}V_2 \tag{2a}$$

$$I_1\frac{1+z^{-1}}{2} = \frac{T}{L_a}\frac{z^{-1}}{1-z^{-1}}\left(V_1 - \frac{L_a}{L_2}V_2\right) \tag{2b}$$

$$V_2 = \frac{T}{C_2 + C_3 + C_b}\frac{1}{1-z^{-1}}\left(-I_2\frac{1+z^{-1}}{2}\right) + \frac{C_2 + \frac{C_b L_b}{L_a}}{C_2 + C_3 + C_b}V_1 + \frac{C_3 + \frac{C_b L_b}{L_3}}{C_2 + C_3 + C_b}V_3 \tag{2c}$$

$$I_2\frac{1+z^{-1}}{2} = \frac{T}{L_b}\frac{z^{-1}}{1-z^{-1}}\left(V_2 - \frac{L_b}{L_2}V_1 - \frac{L_b}{L_3}V_3\right) \tag{2d}$$

$$V_3 = \frac{T}{C_4 - C_L + C_3 + C_c}\frac{1}{1-z^{-1}}\left(\frac{-V_3}{R_L} - I_3\frac{1+z^{-1}}{2}\right) + \frac{C_3 + \frac{C_c L_c}{L_3}}{C_4 - C_L + C_3 + C_c}V_2 \tag{2e}$$

$$I_3\frac{1+z^{-1}}{2} = \frac{T}{L_c}\frac{z^{-1}}{1-z^{-1}}\left(V_3 - \frac{L_c}{L_3}V_2\right) \tag{2f}$$

where, given the element values from the prototype filter in fig. 1, with T=1.256637:

$$L_a = L_1 // L_2;\quad L_b = L_2 // L_3;\quad L_c = L_3 // L_4$$
$$C_a = \frac{T^2}{4L_a};\quad C_b = \frac{T^2}{4L_b};\quad C_c = \frac{T^2}{4L_c};\quad C_S = \frac{T}{2R_S};\quad C_L = \frac{T}{2R_L} \tag{3}$$

A normalized SI structure, using the same integrators used in [1], is shown in schematic form in fig. 5. To that structure must be added the biasing current sources, one for each transistor, with a current proportional to the transistor transconductance. Some method of increasing the ratio among integrator output and input conductance is also necessary [5]. The input circuit is the simplest of the ones presented in [1] to realize the bilinear integration of the input signal. The input can be sampled once at each of the two phases, or once for each period, but it is used only in phase 2. The correct output is available at phase 2, with a delayed copy at phase 1. The circuit is operated by four clock signals, 1, 2, 1' and 2', with the relations shown in fig. 6. It is a two-phases clock signal with two versions of each control signal. The point x is a low impedance line with a voltage high enough to maintain in the saturation region the transistors with drains connected to it. The clock scheme and the switches to point x are necessary for the precise operation of the integrators and delay used [7].

The ratios of the identified transistor transconductances to the

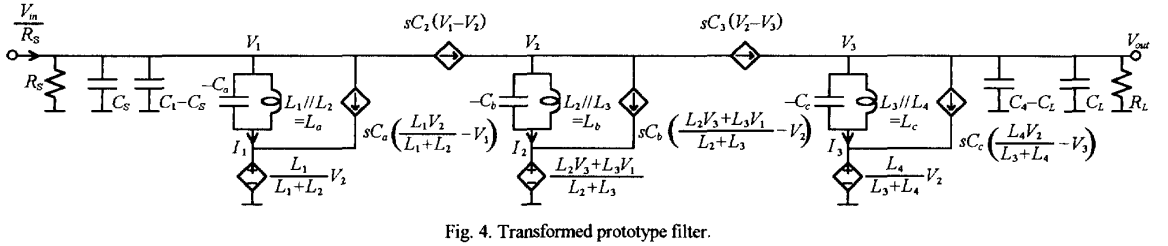


Fig. 4. Transformed prototype filter.

unitary ones (integrator outputs) resulting directly from the equations 2 are also shown. The transconductances of the transistors that form integrator inputs and the current copier at the input circuit are not important, but are assumed as unitary in the simulations.

$M_1 = T/R_S/(C_1 - C_S + C_2 + C_a)$
$M_2 = (C_2 + C_b L_b / L_2)/(C_2 + C_3 + C_b)$
$M_3 = T/L_2$
$M_4 = T/L_a$
$M_5 = T/(C_1 - C_S + C_2 + C_a)$
$M_6 = (C_3 + C_c L_c / L_3)/(C_4 - C_L + C_3 + C_c)$
$M_7 = (C_2 + C_a L_a / L_2)/(C_1 - C_S + C_2 + C_a)$
$M_8 = T/L_2$
$M_9 = T/L_3$
$M_{10} = T/L_b$
$M_{11} = T/(C_2 + C_3 + C_b)$
$M_{12} = T/R_L/(C_4 - C_L + C_3 + C_c)$
$M_{13} = (C_3 + C_b L_b / L_3)/(C_2 + C_3 + C_b)$
$M_{14} = T/L_3$
$M_{15} = T/L_c$
$M_{16} = T/(C_4 - C_L + C_3 + C_c)$
$M_{17} = T/R_S/(C_1 - C_S + C_2 + C_a)/2$
$M_{18} = T/R_S/(C_1 - C_S + C_2 + C_a)/2$

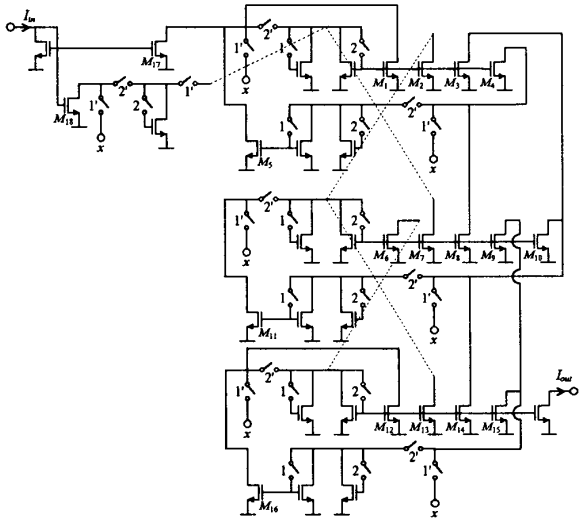


Fig. 5. Schematic representation of an SI realization of a band-pass filter based on Euler integrators.

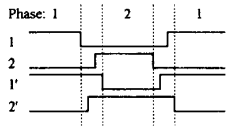


Fig. 6. Switching sequence for the circuit in fig. 5.

IV. BILINEAR SI SYNTHESIS OF BANDPASS FILTERS USING BILINEAR INTEGRATORS

The transformed prototype in fig. 2 can be directly simulated if true bilinear integrators are used. The circuit has only to simulate the *s*-domain modified state equations obtained from the circuit, with bilinear integrators replacing the continuous integrators. This system of modified state equations is (4).

The circuit used in this comparison, shown in fig. 7, was obtained by an adaptation of structures presented in [4] and [5] for polynomial low-pass filters. Note the sampling circuits necessary in the implementation of the direct couplings that realize the finite transmission zeros. The transistor ratios were obtained from eqs. 4, by the same criteria used for the structure in fig. 5. As the input is connected directly, the gain-scaling circuit (factor multiplying V_{in} in eq. (4a)) was moved to the output (M_{17}). This circuit also requires the four-phases switching scheme.

$$V_1 = \frac{T}{C_1 + C_2}\frac{1}{2}\frac{1+z^{-1}}{1-z^{-1}}\left(\frac{V_{in}}{R_s} - \frac{V_1}{R_s} - I_1\right) + \frac{C_2}{C_1 + C_2}V_2 \quad (4a)$$

$$I_1 = \frac{T}{L_a}\frac{1}{2}\frac{1+z^{-1}}{1-z^{-1}}\left(V_1 - \frac{L_a}{L_2}V_2\right) \quad (4b)$$

$$V_2 = \frac{T}{C_2 + C_3}\frac{1}{2}\frac{1+z^{-1}}{1-z^{-1}}(-I_2) + \frac{C_2}{C_2 + C_3}V_1 + \frac{C_3}{C_2 + C_3}V_3 \quad (4c)$$

$$I_2 = \frac{T}{L_b}\frac{1}{2}\frac{1+z^{-1}}{1-z^{-1}}\left(V_2 - \frac{L_b}{L_2}V_1 - \frac{L_b}{L_3}V_3\right) \quad (4d)$$

$$V_3 = \frac{T}{C_4 + C_3}\frac{1}{2}\frac{1+z^{-1}}{1-z^{-1}}\left(\frac{-V_3}{R_L} - I_3\right) + \frac{C_3}{C_4 + C_3}V_2 \quad (4e)$$

$$I_3 = \frac{T}{L_c}\frac{1}{2}\frac{1+z^{-1}}{1-z^{-1}}\left(V_3 - \frac{L_c}{L_3}V_2\right) \quad (4f)$$

$M_1 = T/(2L_2)$
$M_2 = T/(2L_3)$
$M_3 = T/(2R_S(C_1 + C_2))$
$M_4 = T/(2L_a)$
$M_5 = T/(2L_2)$
$M_6 = T/(2L_b)$
$M_7 = T/(2L_a)$
$M_8 = T/(2L_c)$
$M_9 = T/(2(C_1 + C_2))$
$M_{10} = T/(2(C_2 + C_3))$
$M_{11} = T/(2(C_3 + C_4))$
$M_{12} = C_2/(C_1 + C_2)$
$M_{13} = C_2/(C_2 + C_3)$
$M_{14} = C_3/(C_2 + C_3)$
$M_{15} = C_3/(C_3 + C_4)$
$M_{16} = T/(2R_L(C_3 + C_4))$
$M_{17} = T/(2R_S(C_1 + C_2))$

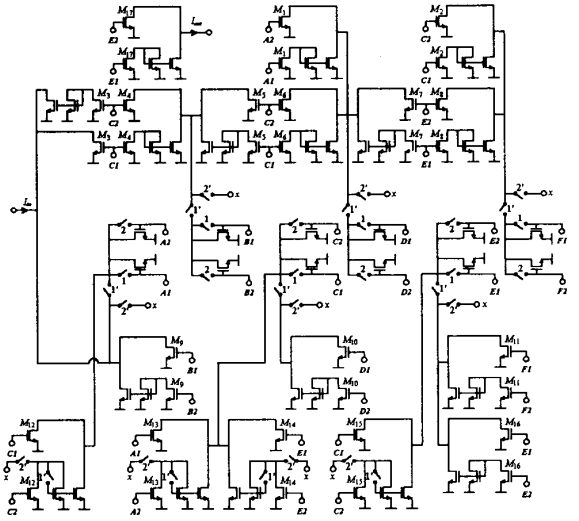


Fig. 7. Schematic representation of an SI realization of a band-pass filter based on bilinear integrators.

V. PERFORMANCE COMPARISON

The first comparison is of sensitivity characteristics. The synthesis using Euler integrators results in the simplest circuit, but the transformations made in the prototype are expected to result in some sensitivity degradation, specially at the high-frequency stopband, where the capacitances added to the prototype filter are more significant. The synthesis using bilinear integrators results in a larger circuit, and the circuit contains signal subtractors and

several inverters. The subtractors do not appear to be a so serious problem. Even as their function is to create the zeros at $z=-1$ required by the bilinear integrations, curiously the predicted error margin in the high-frequency stopband, close to the half of the switching frequency, is small. The inverters add most of the error, because they use three transistors with the same sensitivity to realize a transconductance. Uncorrelated 5% random errors were considered for all the transconductances (or *W/L* ratios of the transistors). This is rather too high for an actual filter, and the assumption of identical errors is valid only if the errors in the transistor dimensions W and L are negligible. For comparison purposes, however, these assumptions are acceptable.

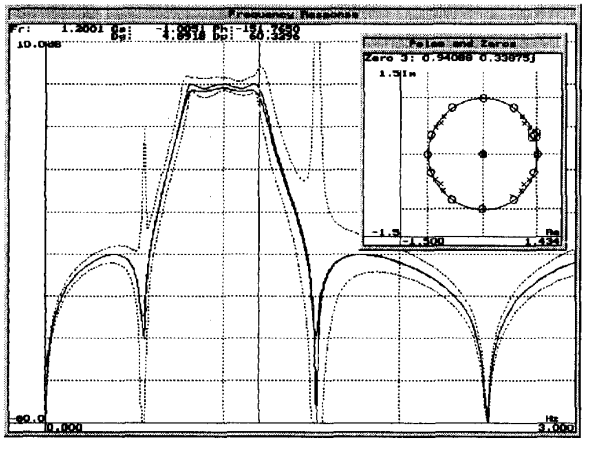


Fig. 8. Gain curves for the filter using Euler integrators. In the smaller window, the poles and zeros of the discrete transfer function in $z^{1/2}$.

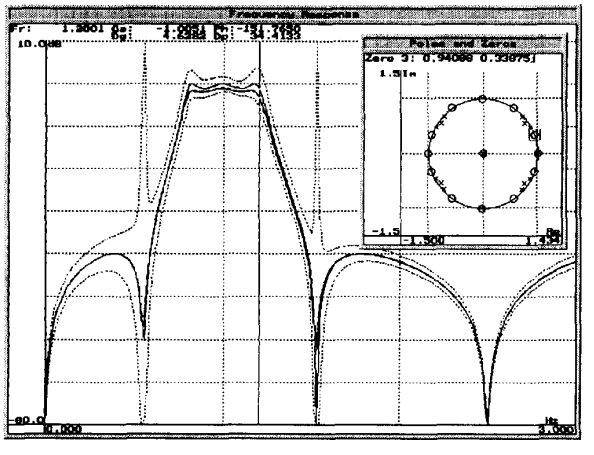


Fig. 9. Gain curves for the filter using bilinear integrators. In the smaller window, the poles and zeros of the discrete transfer function in $z^{1/2}$, the same of fig. 8.

The second comparison criterion is the effect of finite G_m/G_{ds} ratio in the transistors, and parasitic C_{gd} capacitances. For this rather critical filter, some additional circuits for reducing these effects are definitely necessary. The circuits were simulated in the basic form, without enhancement circuits, assuming G_m/G_{ds} and C_{gs}/C_{gd} ratios of 1000, with the biasing and signal current sources assumed as ideal. This is not realistic for the basic structures, but is reasonable when it is assumed that the additional circuits are present. The effects on the two structures are equivalent. The current dynamic range in the structures was not equalized, but this would have little effect in the sensitivity to errors and imperfections.

Figs. 8 and 9 show the gain curves with errors computed for the two structures, using the ASIZ program [5]. The dotted lines represent the error margins for the ideal filter, computed as the statistical deviation of the gain. The transistors were considered as ideal current sources in the sensitivity analysis. The curves show the lower sensitivity of the filter with Euler integrators in low frequency, due to the simpler structure, and the advantage of the filter with bilinear integrators at high frequency, due to the better preservation of the prototype sensitivities. The error peaks at the transmission zeros are an artifact of the computation of errors by sensitivity analysis. The solid curves are the ideal one and what results with the imperfections considered. The poles and zeros in $z^{1/2}$ of the ideal discrete transfer function are also shown. The curves represent the transfer function considering only the output at phase 1, scaled for unitary maximum gain (multiplied by 4). The sampling of the output is impulsional, and so what is plotted is the "digital" response.

VI. CONCLUSION

Two methods for the switched-current simulation of a passive ladder band-pass filter were presented and compared. The method using Euler integrators results in the simplest circuit, but that realization is somewhat more sensitive to component mismatches than the filter based on true bilinear integrators. The example used was particularly critical for the structure with Euler integrators, due to the low ratio among switching frequency and passband center frequency. For higher ratios, more practical, the structure with Euler integrators is preferable, because its simplicity counterbalances the lack of perfect sensitivity preservation. The true bilinear structure is probably preferable in a balanced realization, where the inverters would not be necessary, but this remains to be investigated.

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