ELIMINATION OF NONLINEAR CLOCK FEEDTHROUGH IN COMPONENT-SIMULATION SWITCHED-CURRENT CIRCUITS

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ABSTRACT

This paper discusses a technique for the cancellation of clock feedthrough effects in component-simulation switched-current filters, based on a scaled replication of the parts of the circuit that control the filter coefficients. The regular structure of these filters is particularly convenient for the application of the technique, that can also be applied to other structures. As additional benefit, considerable layout simplification can be obtained, because the same technique cancels systematic errors in transistor widths, what allows layouts to be done without splitting the coefficient-controlling transistors in several identical units, as usually done for better matching.

I. INTRODUCTION

The technique that we call "component-simulation" for the design of switched-current analog sampled-data filters [1] is described in detail in [2][3][4]. Essentially, it consists in the replacement, in a transconductor-C filter, of the transconductors and capacitors by switched-current equivalents, derived by the application of s-to-z transformations to the system of nodal equations describing the filter. Particularly, the application of the bilinear transformation:

$$s \rightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{1}$$

to the nodal system:

$$s\mathbf{C}\mathbf{v}(s)+\mathbf{G}\mathbf{v}(s)+\mathbf{i}(s)=\mathbf{0} \tag{2}$$

results in:

$$\left(1-z^{-1}\right)\frac{\mathbf{C}}{T}\tilde{\mathbf{v}}(z)+\left(1+z^{-1}\right)\frac{\mathbf{G}}{2}\tilde{\mathbf{v}}(z)+\left(1+z^{-1}\right)\frac{1}{2}\tilde{\mathbf{i}}(z)=\mathbf{0} \tag{3}$$

The required z-transform transfer functions can all be obtained as switched transadmittances, from the generic circuit in fig. 1. It is operated by two switches controlled by nonoverlapping clock signals, in a two-phases system where the circuit performs the same operation in both phases. Considering that z^{-1} is a delay from one phase to the other, its transfer function is:

$$I=(G+H+z^{-1}H)V \tag{4}$$

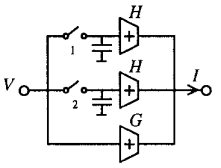

Fig. 1. Generic switched transadmittance.

As explained in [2][3][4], the best realizations are obtained with the use of modulated signals, that is: at the input and at the output of the filter, modulators that invert the polarity of the signal at each phase are inserted. This has the effect of inverting the signal of z in the filter transfer function, as shown in fig. 2.

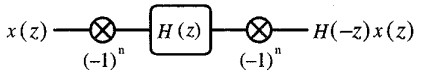

Fig. 2. Modulation and demodulation process.

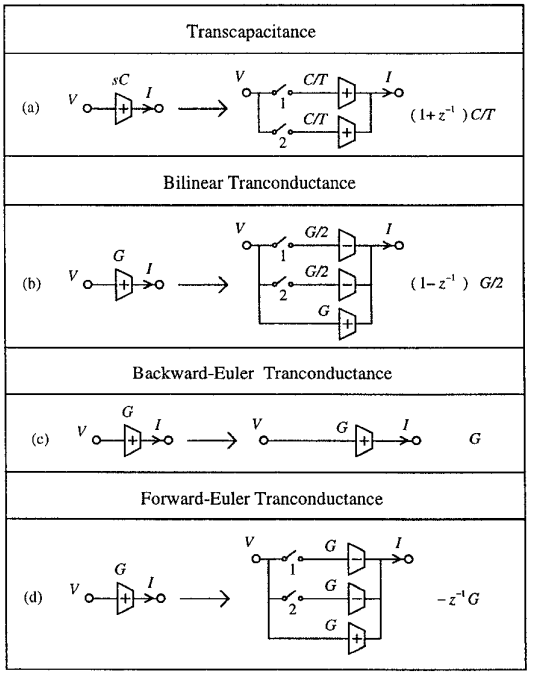

Table 1. Transconductances and transcapacitances for the usual s-to-z transformations.

Table 1 shows the switched transadmittances that correspond to transconductances and transcapacitances after the application of the bilinear and the two Euler transformations to eq. (2). Note that capacitors can always be simulated by transcapacitances (one for a grounded capacitor and four for a floating capacitor), and that, if the input and the output of the circuit are in current, the interconnections of these blocks satisfy the requirements for nonlinearity cancellation of switched-current filters (structures based on current mirrors).

A lossy integrator, for example, would be built as shown in fig. 3, with possible simplifications in the switches and inverters, and implementation with single-transistor transconductors shown. More complex filters, derived from LC doubly-terminated passive prototypes through their Gm-C simulations, are extensions of the same idea [2][3][4]. This example has only one "node" (the input). More complex circuits would have several "nodes" like this, all composed of an input current inverter, a pair of switches, and three series of transistors acting as transconductors.

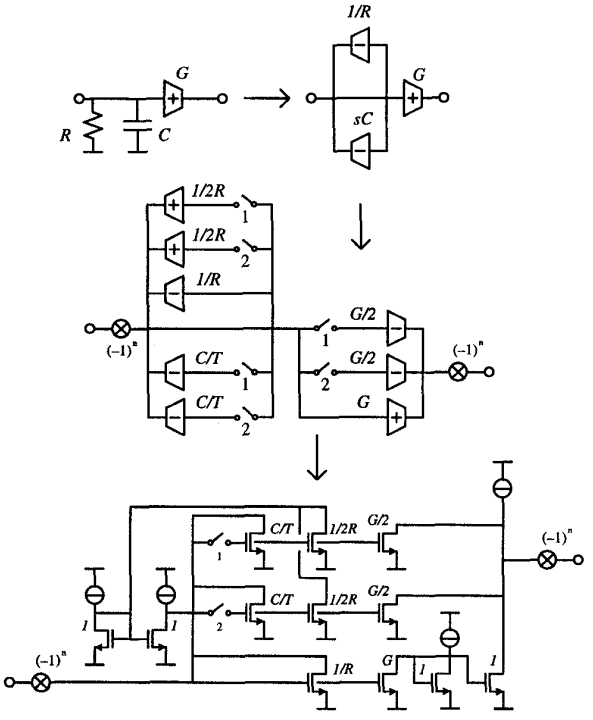

Fig. 3. "Modulated" component-simulation implementation of a lossy bilinear integrator.

Component-simulation filters, are sensitive to charge injection by clock feedthrough in the switches, that can cause nonlinear distortion, because the injected charges affect the input voltages of the transconductors, that have a nonlinear relation with their drain currents. The "modulated" version would reject the injection if its effects were linear, because identical injections would occur at successive phases, changing the direct and the inverted versions of the signal in the same way, what cancels out the effect. Due to the signal dependency of the clock feedthrough, however, some special circuitry is still required for the effective control of this parasitic effect.

In this paper, we propose a method for the cancellation or reduction of clock feedthrough effects in these circuits, using a scaled replication technique. The method also allows substantial simplification on the filter layout, because the replication also cancels the effects of systematic errors in the effective width of the MOS transistors that control the filter coefficients. A precise filter can be obtained without splitting the coefficient-controlling transistors in many small units, as usually done for better matching.

II. NONLINEAR CLOCK FEEDTHROUGH COMPENSATION IN COMPONENT-SIMULATION STRUCTURES

The charge injection through the switches occurs at the opening of the switches, at the end of each phase. This causes the stored currents in the transistors with gates connected to switches to be altered to incorrect values, in a way that depends on the signal current, causing distortion.

Searching for an adequate compensation scheme, we first considered an adaptation of the S^2I technique [1], that consists in making an additional sampling after the opening of the main switches, in a way that stores the error caused by the clock feedthrough, passing to the next phase a compensating current that cancels the error. The application of the idea to these circuits, however, proved to be too complex, due to the presence of unswitched transconductors in the circuit, and to the symmetry from phase to phase of the component-simulation circuits.

We found a very effective technique using scaled replication of the transconductors that implement the filter coefficients. The idea is illustrated in fig. 4, for the lossy integrator in fig. 3.

All the transistors that control the filter coefficients have their widths multiplied by a factor $1+\alpha$, and are duplicated, with the copies having the widths multiplied by α. The factor α can be a fraction or 1. The copied transconductances have their polarities inverted, and so the circuit function remains the same. In the structure shown (as in any component-simulation structure), a polarity inversion is accomplished by simply connecting the transconductor outputs to the current inverter that is at the input of the destination "node". The switches are also duplicated, but are not scaled.

If a switch with a given fixed size is connected to a transistor with fixed length and width W, the change in the transistor drain current, ΔI_d, due to a clock variation ΔV_{clock}, can be, in an approximation considering that the effect is caused by a capacitive divider, as:

$$\Delta I_d \cong \Delta V_{clock} \frac{Cgs_{switch}}{Cgs_{gm} + Cgs_{switch}} Gm \cong \Delta V_{clock} \frac{Cgs_{switch}}{Cgs_{gm}} Gm$$
$$\cong \Delta V_{clock} \frac{Cgs_{switch}}{K_1 W} K_2 W = \Delta V_{clock} \frac{Cgs_{switch}}{K_1} K_2 \quad (5)$$

where we consider that the transistor input capacitance and the transistor transconductance are proportional, by the factors K_1 and K_2, to its width W. Note that the current change is independent of W if the input capacitance is sufficiently greater than the switch capacitance.

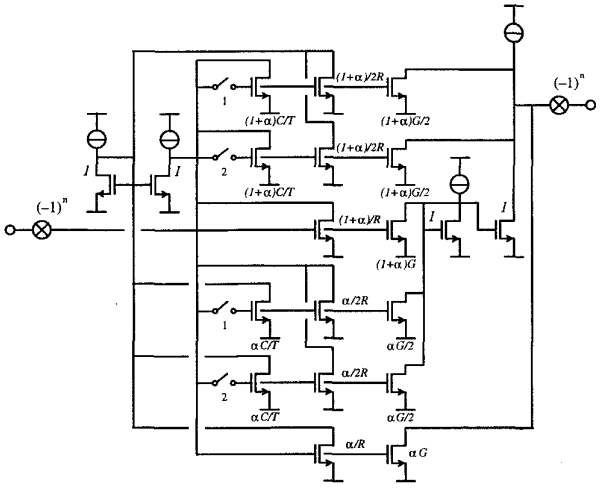

Fig. 4. Lossy bilinear integrator with clock feedthrough compensation by scaled replica.

In the proposed scheme, the transistors in the original circuit and in the replicated circuit operate with exactly the same signals, and so their signal-dependent incremental input capacitances and transconductances have the same values in both circuits. The current changes caused by clock feedthrough in the switches in both circuits are approximately identical, are subtracted in the input current inverter circuit, and so canceled.

Due to the identical operating conditions of the original circuit and of the replica, good cancellation is expected even when more complex models are considered. In any case, if identical charges are injected in the input capacitances of the transistors by the switches, the current changes in the transistors are canceled.

The factor α can be small, maybe around 0.2, and so the required extra area and power are not so significant. An additional consideration, discussed in the next section, can make use of the technique to reduce substantially the area required for the layout of the circuit.

III. LAYOUT WITHOUT TRANSISTOR SPLITTING

It is usual practice in the layout of precise SI filters to split the transistors that control the filter coefficients in several small identical units, to avoid inaccuracies due to bad matching of transistors with different sizes. Considering that there are significant distances that have to be maintained between any two separate transistors, and the area required for their interconnections, this may cause significant increase in the silicon area required for the filter.

If the transistors are all of the same length, the main reason for the mismatch among different transistors is the imprecision in the extremities of their widths. In a typical case, an approximately constant width variation would appear in all the transistors. Note that the width of a MOS transistor in a typical integration process is significantly less precise than the length.

If the scaled replication technique is used, without splitting the transistors, any constant width variation added to all the transistors, in the original circuit and in the scaled replica, has its effect canceled due to the current subtraction performed by the input circuits of the "nodes", effectively eliminating most of the mismatch problem. The current gain of a current mirror that should be W_2/W_1, that normally would present an error due to systematic boundary effects becoming $(W_2-\Delta)/(W_1-\Delta)$, with the scaled replication becomes:

$$A_i = \frac{(W_2(1+\alpha)-\Delta)-(\alpha W_2-\Delta)}{(W_1(1+\alpha)-\Delta)-(\alpha W_1-\Delta)} = \frac{W_2}{W_1} \quad (6)$$

IV. EXAMPLE

To illustrate the basic idea of the scaled replication technique, we performed some simulations using the model shown in fig. 5. Two transistors with widths $W(1+\alpha)$ (M_1) and $W\alpha$ (M_2) are connected through identical switches with their gates connected to switches, connected to a common voltage V_{in}. The transistors are biased by identical voltage sources V_{dd1} and V_{dd2}. The control transistor M_3 has a width W, and is biased with the same voltages. The current through M_3 is measured as the current through V_{dd3}, and used to control the two CCCSs, that have current gains $A_{i1}=1+\alpha$ and $A_{i2}=\alpha$, respectively. With this connection, and the switches closed, the currents through V_{dd1} and V_{dd2} are initially zero, and are changed to an amount corresponding to the charge feedthrough error when the two switches are opened. The correct operation of the technique would result in nearly identical currents in both voltage sources after the opening of the switches, for any value of V_{in} any fall time of the clock signal.

Here we present just one of the possible situations, with $\alpha=1$. $V_{dd1}=V_{dd2}=V_{dd3}$ were set to 2 V, with V_{in} also set to 2 V. The transistors were sized as 2 μm x 1.2 μm for the NMOS switches and 50 μm x 4.8 μm for M_3. M_1 is composed by two transistors identical to M_3 in parallel (otherwise adjustments would be necessary in the current gains to compensate for boundary effects), and M_2 is identical to M_3.

The clock signal was considered as varying from 0 to 5 V, with rise and fall times of 1 ns. The parameters used were taken from the AMS 1.2 μm CMOS process, and the simulations were run with HSPICE.

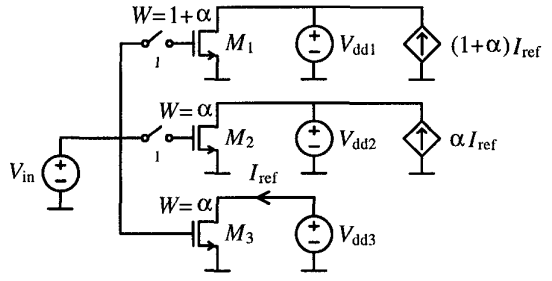

Fig. 5. Model used in the evaluation of the current replication technique.

The simulations show the expected effect, with the final error being of just 0.2 μA (fig. 8) over the 460 μA that is the current in M_3 with this biasing. Without the technique, the clock feedthrough error would amount to about 8 μA (fig. 7). Part of these values can be predicted with just a linear reasoning: the switches have an area 100 times smaller than the area of M_3. Considering the effect of half of the switch capacitance and an effective clock signal excursion of 2 V (with less than about 3 V the switches are closed), the voltage variations at the gates of M_1 and M_2 would be 2/401=0.499 mV and 2/201=0.995 mV respectively, what agrees approximately with fig. 6. The final current error is more difficult to predict, as it depends on small variations in the transconductances caused by the small difference in the gate voltage variations and other parasitic effects, and is the main source of nonlinearity.

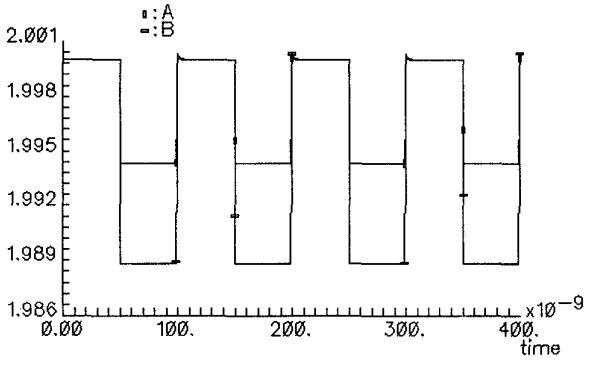

Fig. 6. Gate voltages for M_1 (A) and M_2 (B).

V. CONCLUSION

The application of a clock feedthrough compensation technique to component-simulation SI circuits was presented. The technique is effective, attenuating significantly the linear and the nonlinear parts of the clock feedthrough interference. The proposed implementation does not necessarily increase the power consumption of the circuit, because due to the clock feedthrough cancellation, the current memory transistors can be made smaller than in a normal circuit, with more voltage clock feedthrough at their gates acceptable. Additionally, the technique can be used to reduce the silicon area required for the filter, by eliminating the main reason for the splitting of transistors in several unit parts when implementing precise current mirrors, that is the presence of systematic width errors in the transistors.

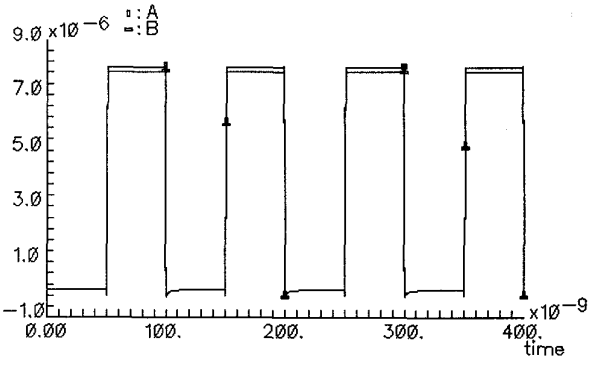

Fig. 7. Currents through V_{dd1} (A) and V_{dd2} (B).

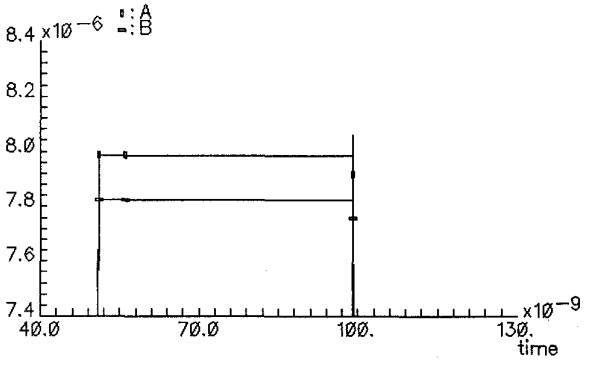

Fig. 8. Expansion of an area of fig. 8, showing the final error as the difference between the two currents.

REFERENCES

[1] C. Toumazou, J. B. Hughes, and N. C. Battersby, eds. *"Switched-Currents, an Analogue Technique for Digital Technology,"* London: Peter Peregrinus Ltd., 1993.

[2] J. Schechtman, A. C. M. de Queiroz, and L. P. Calôba, *"Switched-current filters using component simulation,", Proc. 1994 IEEE ISCAS,* London, England, pp. 569-572, May 1994.

[3] J. Schechtman, A. C. M. de Queiroz, and L. P. Calôba, *"A practical implementation scheme for Component Simulation SI filters," Proc. 38th MWSCAS,* Rio de Janeiro, Brazil, pp. 174-177, August 1995.

[4] J. Schechtman, A. C. M. de Queiroz, and L. P. Calôba, *"Switched-current filters by component simulation",* Analog Integrated Circuits and Signal Processing, pp. 303-309, July 1997.