AUTOMATIC ADJUSTMENT OF THE OUTPUT IMPEDANCE OF A BALANCED TRANSCONDUCTOR USING A CHARGED CAPACITOR

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Abstract - *This paper describes an automatic tuning method that can adjust the output impedance of a balanced transconductor to infinity. The method uses a charged capacitor connected across the output of a master transconductor with zero input voltage. As the voltage over this capacitor increases or decreases exponentially if the output impedance of the transconductor is negative or positive, a control loop setting this voltage to a fixed value also sets the output impedance of the transconductor to infinity.*

Index Terms - Automatic tuning, Q tuning.

I. INTRODUCTION

Transconductor-C filters using balanced transconductors without internal nodes were introduced some time ago [1][2], as a method that could generate continuous-time filters for operation at very high frequencies. One of the characteristics of these transconductors is that their output impedance is set to infinity by a parallel connection of structures that generate positive and negative output impedances, and that also provide common-mode cancellation by presenting a low resistive load to common-mode signals.

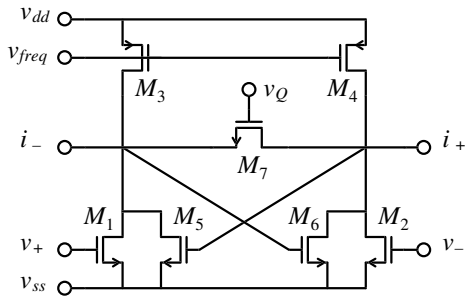

FIGURE 1
A SIMPLE BALANCED CMOS TRANSCONDUCTOR WITH COMMON-MODE CANCELLATION.

Fig. 1 shows the balanced transconductor proposed in [2], that will be used as example in this paper. M_1 and M_2 form the balanced transconductor, with input v_+-v_-, biased by the current sources M_3 and M_4. M_5 and M_6 form a negative resistance across the output i_+-i_-, and M_7, operating in the Ohmic region, forms a positive resistance that shall cancel the negative resistance. M_5-M_6 also form resistances to ground for common-mode signals. The control voltage v_{freq} adjusts the transconductance of the device, and so the operating frequency of the filter, and the control voltage v_Q adjusts the output impedance. In normal operation, v_{freq} is connected to an automatic frequency tuning system, and v_Q to another automatic Q-tuning system. In the usual configurations, the Q tuning voltage is obtained by a control system that adjusts the quality factor of a master resonator to a specified value.

II. AUTOMATIC TUNING OF THE OUTPUT IMPEDANCE USING A CHARGED CAPACITOR

Automatic Q tuning adds some undesirable complexity to the circuit, and if implemented by measuring the Q of a resonator, usually requires rectifiers and a smoothing filter in the control voltage, to avoid interference with the regular operation of the filter (automatic frequency tuning, if left operating all the time, also has this problem). Another problem is possible interference between the frequency and Q tuning systems, both operating with AC signals. In many cases, the use of transconductors without internal nodes is enough to guarantee a good frequency response in the transconductances, and all that remains to be adjusted are the output impedances of the transconductors.

A curious method for this objective departs from the observation that the output conductance of a transconductor as the one in fig. 1, when properly adjusted for almost zero value in a nonzero output voltage range, is negative at the central portion of the range, becoming positive at the edges [2]. This is a consequence of the limited output voltage range, and of the imperfect matching between the nonlinearities of the negative resistance made by the crossed transistors M_5-M_6 and the positive resistance made by the transistor in the Ohmic region M_7. A capacitor connected across the output would stabilize with a voltage delimited exactly by the two limits where the incremental output conductance changes signal. If the voltage is smaller than the limit, the capacitor sees a negative conductance and its voltage increases. If the voltage is larger, it sees a positive conductance and its voltage decreases.

A control system can then be built that measures the voltage over a capacitor connected across the output of a master transconductor, and adjusts the control voltage v_Q, applied also to all the transconductors in a slave filter, until the volt-

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age is at a certain reference level. This would adjust the width of the region where the output conductance is slightly negative, and so adjust the range where the average output conductance of all the transconductors is zero. Fig. 2 shows a possible implementation: C_1 is the capacitor connected across the output of the master transconductor, that has its input at the common-mode voltage v_{cm} of the system. As the voltage over C_1 can have any polarity, a comparator senses the polarity and switches on just one of the two single-ended transconductors with transconductances *Gm*. Of the output current of the selected transconductor is then subtracted a reference current *i*, and the resulting current is applied to the integrating capacitor C_2. R_2 is a "lead" compensation to stabilize the control loop, as seen below.

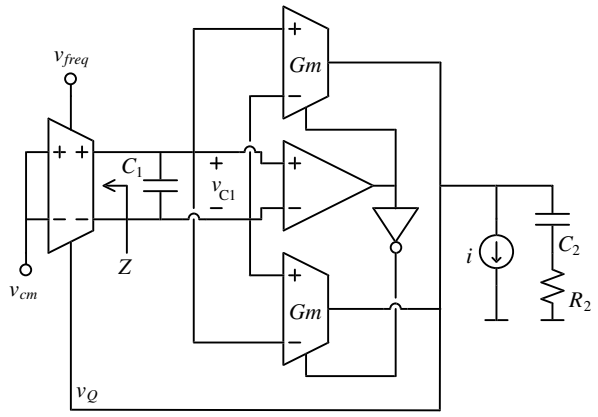

FIGURE 2
OUTPUT IMPEDANCE CONTROL CIRCUIT.

The capacitor C_1 will stabilize with a voltage $v_0 = i/Gm$, with any of the two possible polarities. The dynamic behavior of the control loop is nonlinear, but can be linearized if small variations are assumed, as in the following analysis:

Starting from the time $t = 0$, The voltage over the capacitor C_1 has approximately the form:

$$v_{C_1}(t) = v_{C_1}(0)e^{-t/(ZC_1)} \tag{1}$$

where *Z* is the output resistance of the transconductor. This equation can be further approximated, assuming *t* small, as:

$$v_{C_1}(t) = v_{C_1}(0)\left(1 - \frac{t}{ZC_1}\right). \tag{2}$$

This is the voltage that would be obtained with an integration of a fixed signal "1/Z" with gain $-v_{C_1}(0)/C_1$. Assuming the system close to the stabilization point, $v_{C_1}(0) \approx v_0 = i/Gm$, and so:

$$v_{C_1}(t) \approx v_{C_1}(0) - \frac{v_0}{C_1}\int_0^t \frac{1}{Z(t)}dt \tag{3}$$

or:

$$V_{C_1}(s) \approx -\frac{v_0}{sC_1}\frac{1}{Z(s)} \tag{4}$$

where "*Z*(*s*)" is a Laplace transform version of the parallel combination of the negative resistance formed by M_5-M_6 and the resistance made by the transistor M_7. 1/*Z* can be approximated as:

$$\frac{1}{Z} \approx 2K\frac{W_7}{L_7}\left(v_Q - v_{cm} + \frac{v_0}{2} - V_t\right) - \frac{Gm_5}{2} \tag{5}$$

where *K* and V_t are process parameters, W_7 and L_7 are the dimensions of M_7, and Gm_5 is the transconductance of the transistors M_5 and M_6. v_{cm} is the common-mode voltage at the output of the master transconductor. With all these approximations the circuit is then linearized, and the following relation can be obtained, considering V_Q,V_{cm},V_0,V_t, Gm_5 and *I* as the Laplace transforms of the corresponding signals or constants:

$$V_Q = \left(\frac{1}{sC_2} + R_2\right)\left(Gm\left(-\frac{v_o}{sC_1}\frac{1}{Z(s)}\right) - I\right) =$$
$$= \left(\frac{1}{sC_2} + R_2\right)\left(Gm\left(-\frac{v_o}{sC_1}\left(2K\frac{W_7}{L_7}\left(V_Q - V_{cm} + \frac{V_0}{2} - V_t\right)\right) - \frac{Gm_5}{2}\right)\right) - I\Bigg). \tag{6}$$

From this equation, after some simplification, it is seen that the dynamic behavior of the control loop is governed by the characteristic equation:

$$s^2 + 2K\frac{W_7}{L_7}\frac{Gm\,v_0}{C_1}R_2 s + 2K\frac{W_7}{L_7}\frac{Gm\,v_0}{C_1C_2}. \tag{7}$$

Assuming complex roots, the system resonates at a frequency f_0, with quality factor *Q:*

$$f_0 = \frac{1}{2\pi}\sqrt{2K\frac{W_7}{L_7}\frac{Gm\,v_0}{C_1C_2}}\ \text{Hz}$$
$$Q = \frac{1}{R_2}\sqrt{\frac{1}{2K\frac{W_7}{L_7}\frac{Gm\,v_0}{C_1}C_2}}. \tag{8}$$

An important observation is that the common-mode voltage v_{cm} is dependent on the transconductance adjustment in the transconductor in fig. 1. A correct v_{cm} can be obtained if the master transconductor is biased by another identical transconductor, with inputs and outputs interconnected. See fig. 3. The control loop would work correctly with a fixed v_{cm}, but any nontrivial slave circuit, with variable common-mode voltage, would not follow the master correctly if the transconductance is changed without this biasing. The oscil-

lator shown at the end of the article, for example, only works correctly if the master transconductor is biased in this way.

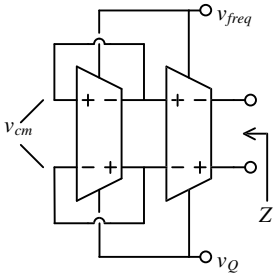

FIGURE 3
BIASING OF THE MASTER TRANSCONDUCTOR.

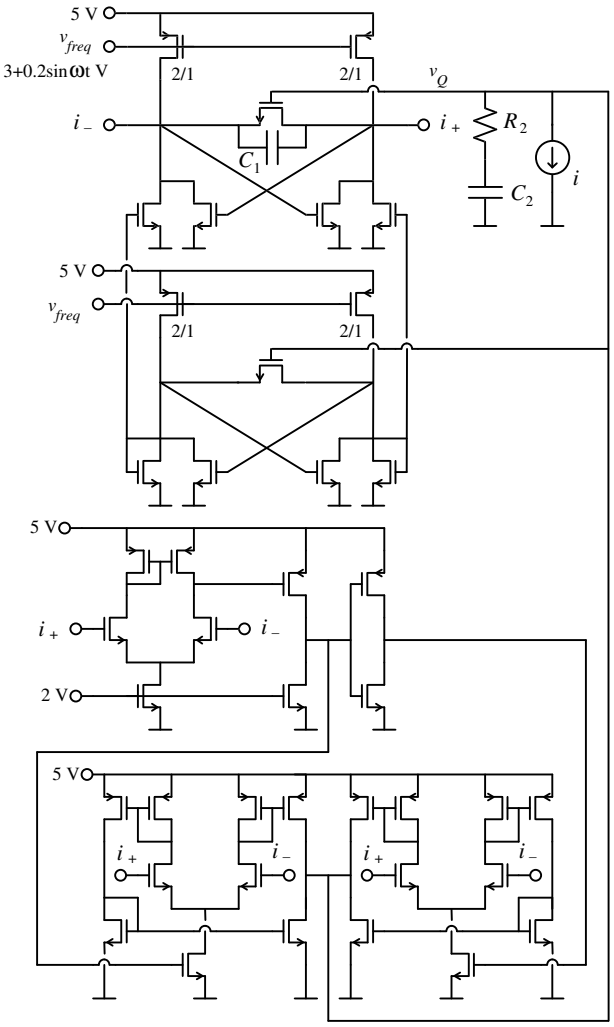

FIGURE 4
SIMULATED CIRCUIT.

III. EXAMPLE

As an example to verify the validity of the analysis, a tuning system implemented in CMOS technology was simulated. The circuit schematic can be seen if fig. 4. The balanced transconductor of fig. 1 is at the top of the drawing, followed by an identical biasing transconductor, a comparator and an inverter, and at the bottom are the two transconductors *Gm*. All the unmarked transistors have a 1/1 aspect ratio. The circuit could be simplified, but in this way the roles of the several components are easier to identify.

As the example is mostly qualitative, no particular realistic technology or optimized design was used. The parameters that appear in (7) and (8), in the example resulted as:

$K = 0.0001$ A/V^2
$C_1 = C_2 = 10$ pF
$W_7/L_7 = 1$
$Gm = 0.00014$ A/V
$v_0 = 0.1$V.

The other values that appear in the equations are:

$V_t = 1$ V
$v_{cm} = 2$ V
$Gm_5 = 0.00014$ A/V
$i = 0.000014$ A.

Fig. 5 shows the simulated output voltage × current characteristic of the transconductor, connected as in fig. 4, where the central portion where the sign of the output conductance can be controlled by v_Q can be observed.

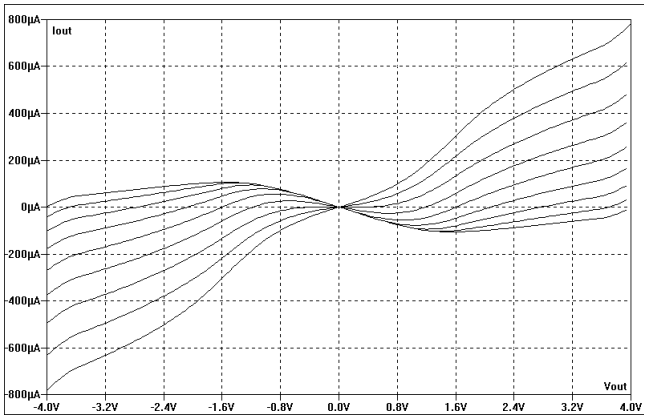

FIGURE 5
SIMULATED OUTPUT CHARACTERISTIC, FOR v_Q VARYING BETWEEN 2 V AND 4 V.

Fig. 6 shows the simulated response in SPICE, with R_2 short-circuited. The circuit really oscillates with a period close to the expected $1/f_0 = 1.18$ µs. The eventual stabilization is due to losses in the circuit, as the nonzero output conductance of the transistors making the transconductors *Gm*, with λ set to 0.05. The simulation was set up with the transconductance of the master transconductor varying sinusoidally at 100 kHz (by changing v_{freq}), to see how the circuit behaves when the frequency tuning is operating, and with a sudden polarity reversal at the capacitor C_1 after 10 µs (v_{C1}

remains inverted after this in the simulations, with the operating *Gm* transconductor changing). A curious fact is that the initial portion of the simulation shows C_1 with initial voltage zero, but this is an artifact of the simulation, since this condition is unstable with v_Q low and M_7 cut off. The voltage grows exponentially after some time, excited only by roundoff errors in the simulation, until M_7 is activated.

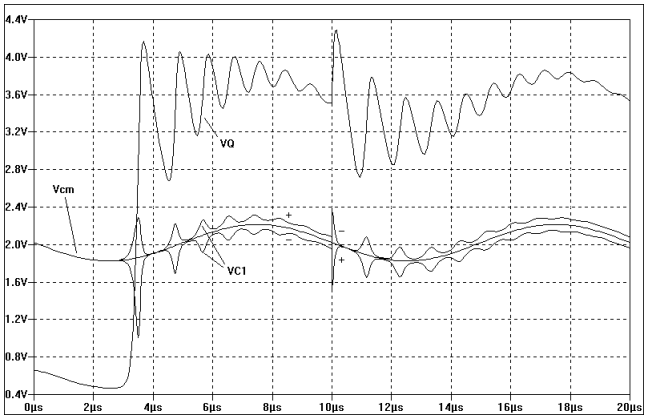

FIGURE 6
SIMULATED BEHAVIOR OF THE Q-TUNING WITH R_2=0.

For Q = 1/2, (8) gives R_2 = 37606 Ω. With this value the behavior of the control loop is as shown in fig. 7. There is no oscillation, as predicted. The value of R_2 is not critical.

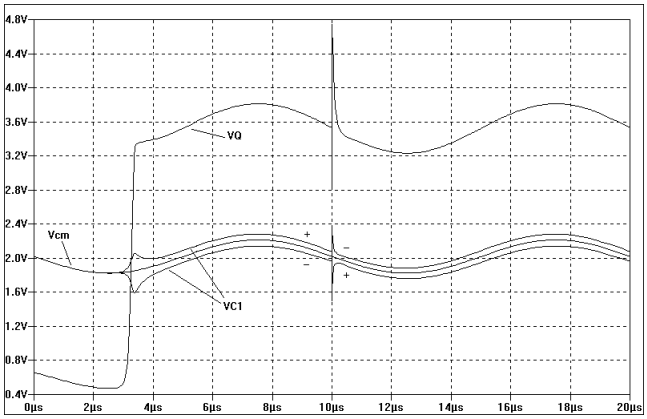

FIGURE 7
SIMULATED BEHAVIOR OF THE Q-TUNING WITH R_2=37606 Ω.

To further verify the reliable operation of the control system, a simple Gm-C quadrature oscillator was simulated. A similar oscillator could be part of a frequency-control loop. In this case nothing was added to the oscillator to control its amplitude of oscillation, or to force oscillation at a high amplitude by the inclusion of some positive feedback. It is so expected that the oscillator shall oscillate with voltage amplitudes close to the limit where the sign of the incremental output conductances of the transconductors change sign. Fig. 7 shows the structure of the oscillator. Fig. 8 shows the simulation results with the same *Q*-tuning setup used in the other simulations. The oscillator is started by a voltage pulse in series with one of the capacitors at 4 µs, and the control current i is doubled between 8 µs and 11µs. As the frequency-control voltage changes, the frequency of the oscillation changes as expected. The amplitude of the oscillations results quite uniform, varying slowly with time. The voltage amplitudes follow closely the v_{C1} limits. They don't exactly double when i is doubled due to the nonlinearity of the *Gm* transconductors.

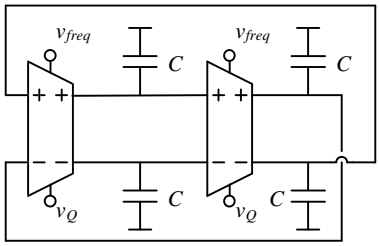

FIGURE 7
TRANSCONDUCTOR-C QUADRATURE OSCILLATOR. C = 40 pF IN THE EXAMPLE.

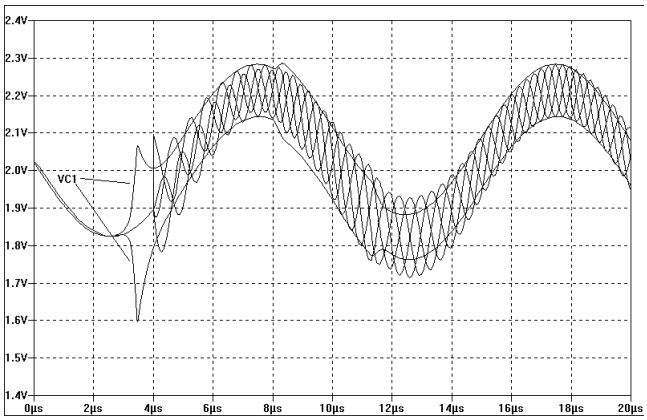

FIGURE 8
SIMULATED OUTPUTS OF THE OSCILLATOR COMPARED WITH THE VOLTAGES AT THE TERMINALS OF C_1.

IV. CONCLUSION

A different system for *Q*-tuning in a transconductor-C filter was proposed, using a charged capacitor to sense the polarity of the output conductance of a master transconductor. The nonlinear control loop that results is easily approximated by a linearized version, that is precise enough for design purposes.

REFERENCES

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