# SENSITIVITY AND ERROR REDUCTION BY COMPONENT SWAPPING IN SWITCHED-CURRENT FILTERS

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## ABSTRACT

This paper describes a procedure for the simulation of passive filters using switched-current techniques, where sensitivity reduction is obtained by swapping the positions and roles of pairs of identical elements at successive switching periods. The technique can produce significant reduction of sensitivity to element mismatches at low cost in terms of added complexity and without reducing the operating speed of the circuit. The technique is exemplified for application to component-simulation switched-current filters.

## 1. INTRODUCTION

A problem that causes important degradation in the sensitivity characteristics of active filters obtained by the simulation of passive prototypes, is that often a single passive element is simulated by an array of active and passive elements.

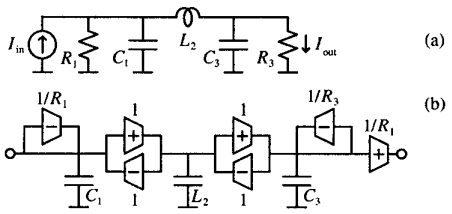


**Fig. 1**. Normalized current-mode *Gm-C* simulation (b) of a polynomial passive filter (a), with optimal sensitivity preservation.

In many cases it is possible to minimize this problem using circuit transformations that map errors in the elements of the active simulation directly to errors in elements of the passive prototype. In this case we can say that the active simulation presents optimal sensitivity preservation. When this happens in a simulation of an *LC* doubly terminated structure designed for maximum power transfer, the gain sensitivities relative to all the elements go to zero at the frequencies of maximum power transfer (with the exception of the terminations, that have sensitivities equal to $\pm 0.5$ at these frequencies, and other extra elements that affect only the flat gain).

For example, consider the current-mode *Gm-C* simulation of a 3rd-order *LC* doubly terminated low-pass polynomial filter shown in fig. 1. The active simulation results in four transconductors and one capacitor for the implementation of the floating inductor, and two transconductors for the realization of the input resistor.

An analysis of the circuit, however, shows that errors in any of the transconductances are equivalent to errors in the impedance level of the circuits connected at their outputs, or simply to errors in elements or groups of elements of the passive prototype.

In general, any polynomial passive filter easily leads to *Gm-C* simulations with optimal sensitivity preservation, because the added transconductors always "see" at their outputs impedances that exist, possibly scaled, in the prototype.

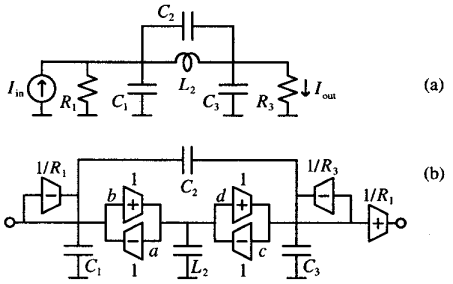


**Fig. 2**. Normalized current-mode *Gm-C* simulation (b) of a passive filter with finite transmission zeros (a), with suboptimal sensitivity preservation.

In the simulation of *LC* doubly terminated filters with finite transmission zeros, a more serious problem occurs, due to the presence of *LC* resonant circuits in the prototype. Fig. 2 illustrates what happens in the simulation of a 3rd-order *LC* doubly terminated filter with a pair of $j\omega$-axis transmission zeros. Due to the presence of $C_2$, It is not anymore possible to say that errors in the transconductors forming the gyrator that connect the capacitor $L_2$ to the remaining circuit, simulating the inductor $L_2$ in the passive prototype, correspond to impedance errors in the prototype.

A sensitivity analysis of this type of circuit shows that, at the frequencies where maximum power transfer occurs between the terminations, the gain sensitivities in relation to the transconductors that form the two gyrators form two pairs (*a-b* and *c-d*) with identical magnitudes and opposite polarities, indicating that optimal sensitivity preservation would require perfect matching between the pairs of transconductors *a-b* and *c-d*. This would transform the pairs into true gyrators, that behave as lossless elements, as the other reactive components.

A procedure that can be used to force the matching among these elements is to interchange the pairs of elements to be matched at a fast rate. As the transconductors are memoryless devices, this is basically possible with the introduction of some switches in

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the circuit, controlled by a two-phases clock signal, at a frequency that is high in relation to the filter operation frequency range.

Another possibility, of simpler implementation, is to match the transconductors $1/R_1$-$a$, $b$-$c$, and $d$-$1/R_3$ (If the prototype terminations are unitary). This has the interesting property of requiring only the interchanging of the input connections of the transconductors (the polarities of the nodal voltages may have to be changed for this), and results in similar overall error reduction.

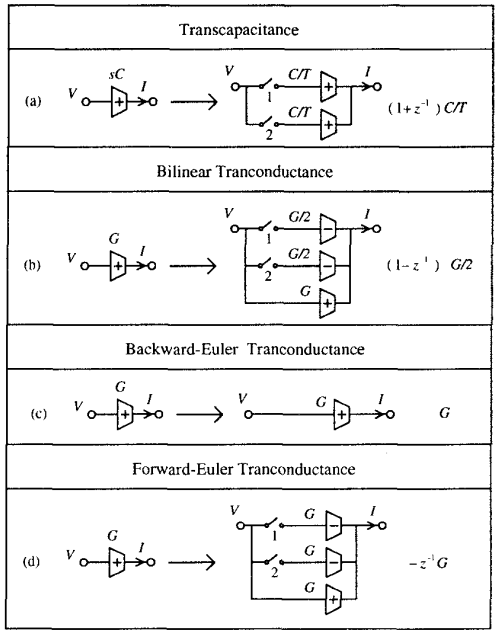


**Table 1.** Transconductances and transcapacitances for the usual $s$-to-$z$ transformations.

More practical implementation forms for the swapping idea can be found in a simple adaptation of the "component-simulation" switched-current technique [1][2][3], to be described in section 2. In this way, the complications of a mixed continuous/switched filter are avoided, and the switching system already present in a switched-current filter is easily adapted.

This "component-simulation" technique transforms any *Gm-C* current-mode filter into a switched-current filter by the simple substitution of continuous-time transadmittances (transconductances and transcapacitances) by equivalent switched-current transadmittances. Table 1 shows the equivalencies using common $s$-to-$z$ transformations for the most practical form of the technique, which works with modulated signals. There are modulators before and after the filter, that invert the polarity of the input and output currents in alternate phases.

The transconductors in table 1 can be as simple as single transistors with bias current sources, but are normally more elaborated, with cascode stages added to increase the output impedance, for example. In this paper the transconductors will be shown implemented by single transistors, to simplify the schematics. The transconductances will be kept normalized.

The *Gm-C* structure in fig. 2(b) is transformed into the equivalent transadmittance circuit shown in fig. 3, where the transconductance and transcapacitance blocks are implemented as in table 1, according to the desired $s$-to-$z$ transformation. The bilinear transformation will be used in this work. The polarities were adjusted to allow the direct interchange of the transconductor pairs $1/R_1$-$a$, $b$-$c$, and $d$-$1/R_3$.

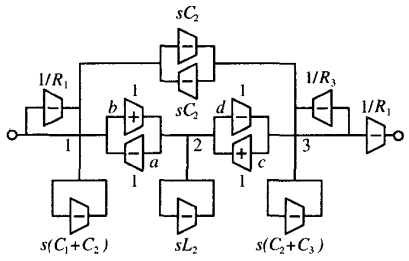


**Fig. 3.** Current-mode transadmittance simulation of the filter in fig. 2.

After switch and inverter simplifications, any component-simulation switched-current filter can be implemented by the interconnection of several "node" blocks comprising one current inverter, two switches, and three series of output transconductors [2]. The circuit in fig. 3 can be implemented as in fig. 4.

## 2. SWITCHED-CURRENT COMPONENT MATCHING TECHNIQUE

The idea is to explore the phase to phase symmetry of the structure, swapping the positions of pairs of transconductors that are to be matched at successive phases. The effect of this in the sensitivities of the filter transfer function in relation to the swapped transconductances is that the new sensitivities are the averages between the two original sensitivities of each pair. The operating speed of the circuit is not changed. Mismatch errors between pairs of elements matched in this way appear mainly as frequency components around one half of the sampling frequency, where they can be easily eliminated by a reconstruction filter, if required.

In the switched-current realization in fig. 4, the transconductors realizing the two gyrators and the terminations correspond now to six sets of three transistors. The equivalent matching requirement for this structure would be the interchange, transistor per transistor, among the pairs corresponding to the original transconductors.

A sensitivity analysis performed by the ASIZ program [4], however, shows that due to the use of the bilinear transformation and to the simplifications made to put all the current inverters at the input of the "nodes", this requirement is somewhat changed. The *Gm-C* transconductors are transformed in such a way that, at the maximum power transfer frequencies, the gain sensitivities relative to the switched parts of the switched transconductors to

be matched are identical and the gain sensitivities relative to the continuous parts are approximately opposite (With the exception of the pair $1/R_1$-$a$, that keeps sensitivities of equal signs in all component pairs, but is included in the process for symmetry). The three transconductor pairs forming the current inverters have exactly opposite gain sensitivities at all frequencies, all zero at DC with the particular set of nodal polarities chosen.

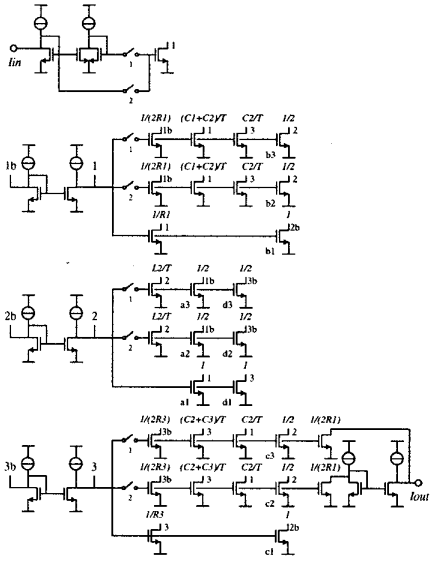


**Fig. 4**. Switched-current component-simulation realization for the circuit in fig. 3. The input modulator is as shown, and the output modulator is incorporated into the output stage.

This means that it is only useful to use the swapping technique with the continuous parts of the gyrator and termination transconductors and with the input current inverters of the nodes. As will be seen, this is also enough for a significant decrease in sensitivity.

The continuous parts of the transconductor pairs $1/R_1$-$a$, $b$-$c$, and $d$-$1/R_3$ have their outputs connected to the same nodes, and so the only necessary change to make them interchange roles is to add pairs of switches to their inputs. This does not happen to the pairs making the input current inverters. The interchange of these elements requires the switching of currents (and a somewhat more complex switching system, similar to the system proposed in [5]), as shown in fig. 5.

**Example:**

Fig. 6 shows simulations with the ASIZ program, comparing the gain statistical deviations for the basic circuit in fig. 4 with the results obtained with the swapping technique. The example filter is a 3rd-order elliptic filter, with Amax=1 dB and Amin=30 dB, and switching frequency (normalized to 1 Hz, corresponding to an effective sampling frequency of 2 Hz) set to 20 times the passband border frequency. The normalized element values are listed in table 2, corresponding to the structure in fig. 2(a).

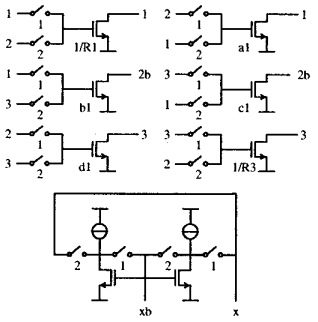


**Fig. 5**. Switching for the swapping of the continuous parts of the switching transconductors pairs $1/R_1$-$a$, $b$-$c$, and $d$-$1/R_3$, and the transconductors forming the three current inverters in fig. 4.

| | |
|---|---|
| $R_1$=1 | $R_3$=1 |
| $L_2$=0.8015 | $C_2$=0.3216 |
| $C_1$=1.7726 | $C_3$=1.7726 |
| T=0.3142 | |

**Table 2.** Element values for the normalized prototype filter in the example.

The curves show the gain error limits predicted by sensitivity analysis in the passband, and the same limits considering the sensitivities discounted from their values at DC, to eliminate from the analysis the errors that affect only the flat gain of the filter (errors in the modulators, and part of the error in terminations and transconductors). An error reduction of about 50% was obtained in the later case, showing the effectiveness of the technique. The sensitivity reduction only doesn't go all the way to the low sensitivity of the passive prototype because nothing was done about the switched parts of the transadmittances.

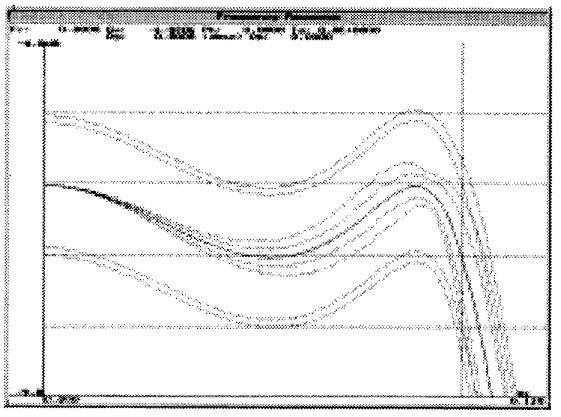

**Fig. 6**.Passband gain statistical deviations for the circuit in fig. 4, considering all elements, assuming 5% variabilities in the transconductances and impulse sampling. The pair of curves closer to the nominal gain curve are computed with sensitivities discounted of their values at DC. The larger limits correspond to the circuit in fig. 4. The smaller limits to the circuit incorporating the matchings by swapping shown in fig. 5. ASIZ screen.

## 3. USING TWO NONOVERLAPPING CLOCK PHASES

The technique has the inconvenience of the need of switching currents for the matching of the current inverters. This impedes a safe operation with only two nonoverlapping clock phases, much as happens in a "second generation" SI circuit [5].

It is possible, however, to circumvent this problem by a modification of the "node" circuit and in the interconnections among them. The idea is to split the transconductances with inputs connected to the "nodes" in two groups, one inverting and one noninverting, each one with its pair of switches, common for all the switched transconductors. Both groups are implemented by inverting transconductors, and at the input point of the "node" there is a "voltage inverter" that goes to the noninverting transconductors, replacing the current inverters of the original circuit. A version of the circuit in fig. 4 using this technique is shown in fig. 7. Note that this new structure preserves the fundamental characteristic of nonlinearity cancellation of switched-current circuits (as well as the one in fig. 4), being based only on current mirrors, where only the W/L ratios of the transistors are important.

The swapping operations shown in fig. 5 are then performed as shown in fig. 8. The new form of the input inverters, that now invert voltage, not current, allows the swapping of the two transconductors that make each inverter without the switching of currents.

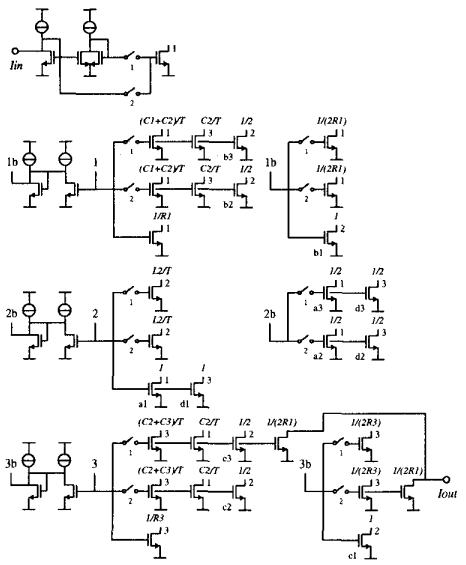


**Fig. 7.** Alteration of the circuit in fig. 4, replacing the current inverters at the input of the "nodes" by voltage inverters, and separating inverting and noninverting transconductors. Note the change in the output modulator.

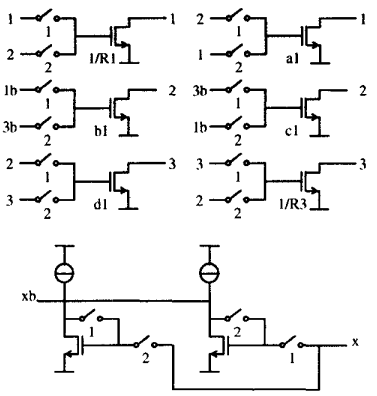


**Fig. 8.** Switching for the swapping of the continuous parts of the switching transconductors pairs $1/R_1$-$a$, $b$-$c$, and $d$-$1/R_3$, and the transconductors forming the three voltage inverters in fig. 7.

The sensitivity performance of the circuit built in this way is exactly the same of the previous circuit (with the swapping operations. The original in fig. 7 has slightly different sensitivity characteristics from the circuit in fig. 4). The circuit can now operate with two nonoverlapping clock phases. Apparently there is an increase in cost due to the larger number of switches (2 per node), but these are small switches that don't have to carry continuous currents.

## 4. CONCLUSIONS

A low-cost technique for the sensitivity reduction in switched filters was proposed, and demonstrated with the component-simulation switched-current technique, that is particularly convenient for its implementation. The same idea can be adapted to other switched-current and switched-capacitor structures, but the implementation may require more than two clock signals if the structure does different operations at each phase.

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