Switched-Current Filters Using Component Simulation

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ABSTRACT

The paper discusses the synthesis of switched-current filters from continuous-time prototypes by the simulation of components, particularly capacitors and transconductors in OTA-C filters. The obtained structures implement discrete-time versions of the nodal equations of the prototype circuit using Euler or bilinear transformations over the circuit elements. All the proposed structures work with doubled effective sampling rate, do not use current-conducting switches, and are operated with a two-phases, non-overlapping clock system.

I. INTRODUCTION

The switched-current (SI) filter designs presented to date have been usually based on state-variable methods using integrators [1, 2, 6] or wave techniques [1, 4]. In this paper a different approach based on a direct simulation of capacitors and continuous transconductors is presented. The obtained structures are equivalent to continuous-time transconductance-C filters, where the continuous elements are simulated by switched-current methods using a Euler or bilinear time discretization formulas. The concept of component simulation is also explored in the "switched-transconductance" technique [1, 5]. The SI filters discussed here are innovative in the aspects that they operate with doubled sampling rate, sampling the input and updating the output at each phase of the switching interval; they are implemented without current-conducting switches, and naturally admit operation with two non-overlapping clock signals. In the "modulated" version, the proposed structures present high immunity to charge feedthrough effects. Several synthesis techniques are possible, all derived from the same basic idea.

II. TIME DISCRETIZATION OF NODAL EQUATIONS

Transconductance-C continuous time circuits can be described by the nodal matricial equation (1). Where **v** is the nodal voltage vector, **G** is the nodal transconductance matrix, **C** is the nodal transcapacitance matrix and **j** is the vector of current sources injected at the nodes.

$$s\mathbf{C}\mathbf{v} + \mathbf{G}\mathbf{v} + \mathbf{j} = \mathbf{0} \tag{1}$$

Several different discretization transformations can be applied to (1) in order to obtain a discrete-time circuit. The usual ones are the bilinear, backward Euler and forward Euler transformations. As example, the application of the bilinear transformation (2) will be used. The procedure is the same for the other transformations.

$$s \rightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{2}$$

After substituting s in the nodal equation (1) and rearranging the result, the following discretized nodal equation is obtained:

$$\left(1-z^{-1}\right)\frac{\mathbf{C}}{T}\mathbf{v} + \left(1+z^{-1}\right)\frac{\mathbf{G}}{2}\mathbf{v} + \left(1+z^{-1}\right)\frac{1}{2}\mathbf{j} = \mathbf{0} \tag{3}$$

Comparing this equation with the continuous time circuit equation (1), the following equivalence of components is obtained:

$$\begin{aligned} sC &\rightarrow \left(1-z^{-1}\right)\frac{C}{T} \\ G &\rightarrow \left(1+z^{-1}\right)\frac{G}{2} \\ j &\rightarrow \left(1+z^{-1}\right)\frac{1}{2}j \end{aligned} \tag{4}$$

Note that transconductances and transcapacitances are mapped into "transconductances with memory". The operation done in the input current can be implemented by a "transconductor" like the ones used for the transconductances. The relations (4) are of simple realization using switched-current circuits.

III. SI "TRANSCONDUCTORS" AND "TRANSCAPACITORS"

Switched-current circuits are built with transconductors (single MOS transistors and bias current sources, in the simplest version) and switches. The transconductors have an input capacitance (gate capacitance) that holds the voltage when the input circuit is at high impedance. This paper discusses only structures were the switches are restricted to be in series to transconductor inputs (transistor gates). In these circuits after a period of stabilization all the currents flowing through the switches became zero. This means that the switches can be opened without perturbation of the general state (ignoring clock-feedthrough effects) and non-overlapping clocks can be used. Taking this restriction into account the desired circuit must be built with two kinds of components: continuous transconductors or switched transconductors (fig. 1).

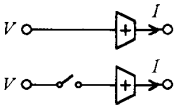

Fig. 1. Continuous (unswitched) and switched transconductors.

Usual switched-current circuits operate with two phases but process the input at only one of the phases. The operating frequency can be doubled if the structures process the input signal at both phases. This can be obtained if there is a structural symmetry from phase to phase.

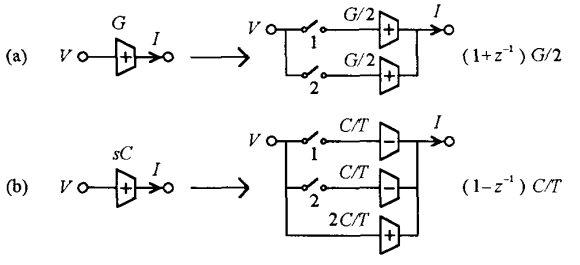

Fig. 2. Bilinear "transconductor" (a) and bilinear "transcapacitor" (b).

Combining the basic components of fig. 1 it is possible to synthesize the components described by the bilinear mapping (4). The bilinear "transconductor" is simulated by 2 switched transconductors (fig. 2a). At each phase one of the switches is closed and the other is open representing a transconductor and a memory of the previous current. The transconductance implemented is $(1+z^{-1})G/2$. Note that z^{-1} here is the delay of one phase (more properly, $z^{-1/2}$ should be used). Since the circuit is symmetric from phase to phase its transference is valid in both phases. The bilinear "transcapacitor" is implemented by noting that $(1-z^{-1}) = 2-(1+z^{-1})$. This relation can be obtained by adding a continuous transconductor to a pair of switched transconductors as shown in fig. 2b. The transconductance obtained is $(1-z^{-1})C/T$. This circuit is also symmetric from phase to phase and the transference is valid in both phases.

The same procedure can be applied to the backward Euler or forward Euler transformations. The "transcapacitors" are the same of the bilinear transformation in both cases. The two Euler "transconductors" are shown in fig. 3a and 3b. These structures can be used to realize LDI simulations [1], or bilinear simulations if convenient transformations are made in the prototype [2, 6].

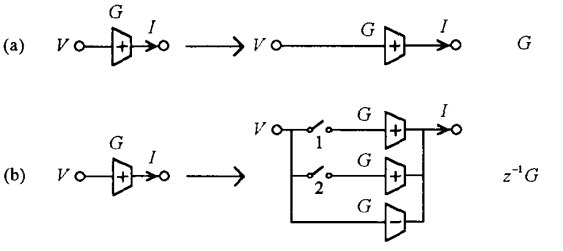

Fig. 3. Backward Euler (a) and forward Euler (b) "transconductors".

Note that all the circuits satisfy the requirements of non-linearity cancellation, that are a characteristic of SI circuits, when interconnected. The input and output of a complete filter must be in current.

IV. SWITCHED-CURRENT CIRCUIT SIMULATION OF OTA-C FILTERS

A direct bilinear simulation of any continuous time circuit made of transconductances and transcapacitances is done by the simple application of the mapping of the continuous-time to the discrete-time components in fig. 2. Fig. 4 shows how to simulate the capacitors of a prototype filter with transcapacitances.

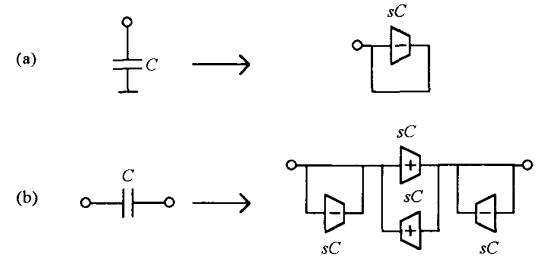

Fig. 4. Grounded capacitor and floating capacitor construction using transcapacitances.

A grounded capacitor is implemented by a negative transcapacitance in closed loop (fig. 4a). A floating capacitor is implemented by the four transcapacitors shown in fig. 4b. Note that an integrator can be constructed by a

transconductor and a capacitor as in fig. 5a or by the simulation of a Miller integrator as in fig. 5b. The later equivalent allows the simulation of conventional RC-active state-variable filters. The amplifier can be as simple as a single grounded-gate MOS transistor amplifier [7]. This structure has the advantage of being more insensitive to the finite output impedances of the transconductors.

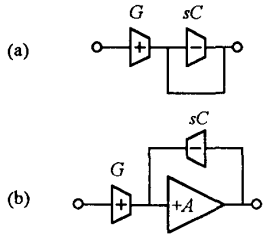

Fig. 5. Integrators: Transconductor-C (a) and Miller (b)

A continuous time transconductance-C circuit of a low-pass 5th order elliptic filter is presented in fig. 6. The circuit is a direct simulation of an LC doubly terminated ladder structure.

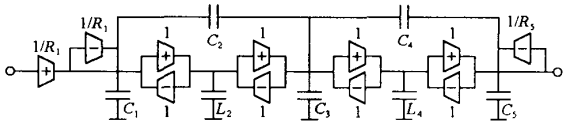

Fig. 6. Schematic representation of a transconductor-C 5th-order elliptic low-pass filter.

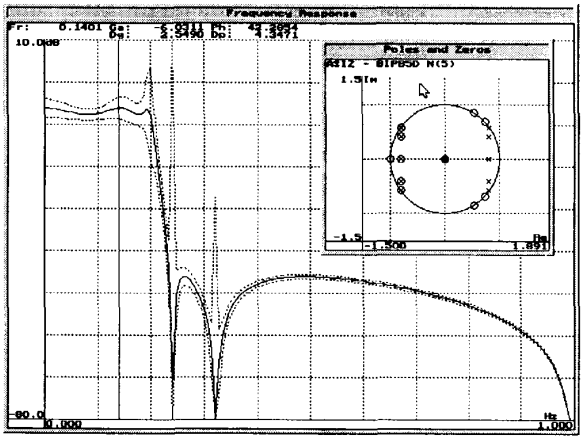

Fig. 7. Gain frequency response of a "normal" bilinear SI low-pass filter, with expected error margins and poles and zeros in $z^{1/2}$.

The transconductance-C circuit can be directly mapped into a switched-current circuit by first expressing the capacitors in terms of transcapacitances (fig. 4) an then applying the bilinear mapping of fig. 2. After the elimination of redundant switches, only two switches for each node of the prototype remain. The frequency response of the switched-current filter is shown in fig. 7. The filter was designed for 1 dB maximum passband attenuation, 40 dB minimum stopband attenuation, and sampling frequency to passband border frequency ratio of 10.

The simulation was made with the ASIZ program [1], with error margins computed by sensitivity analysis, assuming 2% random errors in all the transistor transconductances. The filter was simulated in the most basic form at transistor level, with the transistor output conductances and parasitic capacitances neglected. The negative transconductors were implemented by a single transistor, and the positive transconductors by three transistors.

The result presents a rather high sensitivity to component variations. This is due to the structure of the "transcapacitor" that operates using a cancellation of currents. The effect of a mismatch between the continuous part of the "transcapacitor" and the switched part is to introduce a loss that corrupts the transference. The result is that the loss is higher when the filter has a low cutoff frequency. There is, however, a curious way around this problem. It can be corrected by the use of the "reverse mapping".

V. REVERSE MAPPING AND MODULATION

If the bilinear mapping described by fig. 2 is reversed, that is, the transcapacitances implemented as $(1+z^{-1})C/T$ and the transconductances as $(1-z^{-1})G/2$, the result is the same of a transformation of transconductances into transcapacitances and transcapacitances into transconductances in the continuous prototype filter, and the application of a frequency scaling. A low-pass filter is transformed into a high-pass filter (fig. 8).

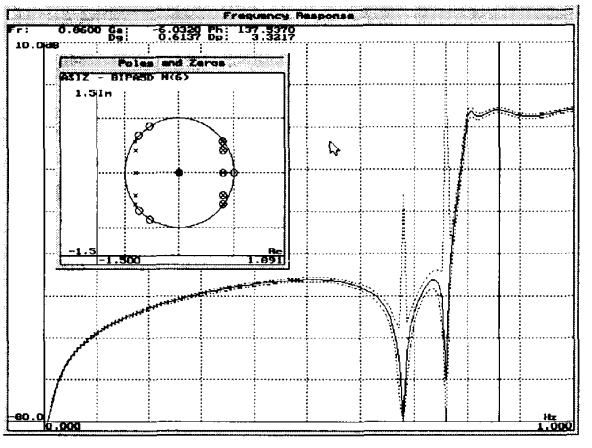

Fig. 8. High-pass filter obtained by the "reverse mapping" of the prototype. The gain frequency response is shown, with expected error margins, and again the poles and zeros. Note the transformation $H(z) \rightarrow H(-z)$.

Note that the sensitivities are much smaller. This occurs because in this case the transition frequency is higher. This high-pass filter is not very useful because it operates near the half of the switching frequency. It can be transformed into a low-pass filter by simply "modulating" the input and output signals of the filter (fig. 9). The modulator is in fact a circuit that changes the sign of the signal at each phase. If $X(z)$ is the input signal of the modulator, the output of the modulator will be $X(-z)$. After the filter $H(z)$ the signal will be $H(z)X(-z)$, and at the output of the second modulator the signal is demodulated becoming $H(-z)X(z)$. The new transfer function is $H(-z)$. This process does not modify the sensitivities and can be used to restore the transference as shown in fig. 10. The result is a low-pass filter with much lower sensitivity that the one obtained by direct transformation. Fig. 11 shows a suitable modulator circuit, that also allows the operation with a two-phases non-overlapping clock.

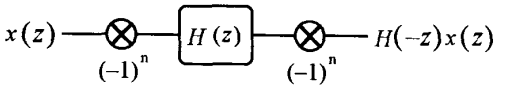

Fig. 9. Modulation and demodulation process.

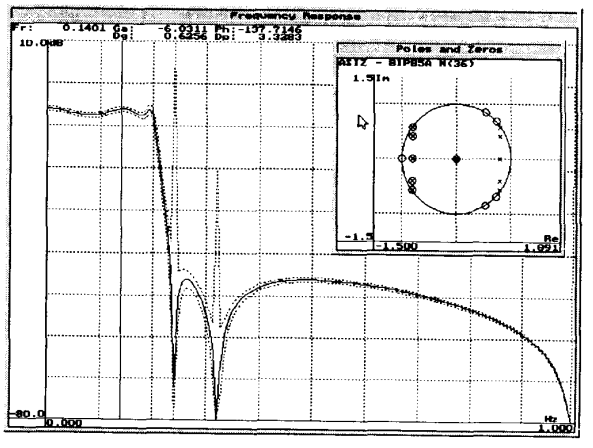

Fig. 10. Low-pass filter gain, error margins, and poles and zeros, obtained by the "modulation" of the input and output signals of the "reverse mapped" example filter.

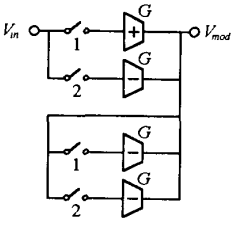

Fig. 11. Modulator circuit, that operates with a two-phases non-overlapping clock.

VI. CONCLUSION

A different technique for synthesis of current-switched circuits was presented. The technique has as the most advantageous characteristics the doubled sampling frequency, that allows for two times faster filters. As the structure uses only switches connected to gates, a simple two-phases non-overlapping clock system is sufficient, with only two switches for each state variable needed. The more complex clocking schemes and extra switches needed for other low-sensitivity structures [3] are avoided. The structures using modulated signals is the least sensitive to component mismatches. It also shows great immunity to clock feedthrough effects, because at successive phases the charge injections at the transconductor inputs are in opposite directions relative to the signal, and so are canceled if non-linear effects are small. The sensitivity characteristics can still be improved with the elimination of the many transistors needed in the implementation of the non-inverting transconductors, what is possible in a fully balanced realization. The example described only the generation of a true bilinear filter. There is also the possibility of building bilinear filters using only Euler integrators [2, 6]. The idea of using modulated signals inside an SI filter can also be extended for other purposes that are under investigation.

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